

INFLUENCE OF WINDOW AND ABSORBER LAYER PROCESSING ON DEVICE OPERATION IN SUPERSTRATE THIN FILM CDTE SOLAR CELLS

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ABSTRACT

Processing strategies are presented for controlling junction quality as both window and absorber layer thickness are reduced in polycrystalline superstrate CdS/CdTe thin-film solar cells. High resistance In_2O_3 and SnO_2 oxide buffer layers improve coverage of chemical bath deposited CdS and device performance with PVD CdTe, resulting in efficiencies $>13.5\%$. A new method of CdS and $\text{Cd}_{1-x}\text{Zn}_x\text{S}$ chemical bath deposition for high Cd utilization and growth rate and low occurrence of adherant particulates is presented. Alloying the CdS film with ZnS can reduce the window thickness tolerance needed to obtain high photocurrent and good junction properties with no oxide buffer layer. CdS diffusion is reduced by annealing in air at 450°C or in argon at 580°C prior to CdCl_2 treatment and by reducing the CdCl_2 and O_2 partial pressures during treatment. Promising device results are presented for CdTe/CdS cells with 1 micron thick CdTe deposited at $T < 400^\circ\text{C}$.

INTRODUCTION

For CdTe/CdS/ITO (or SnO_2)/glass devices, optical absorption in the CdS layer is the predominant photocurrent loss, making it necessary to minimize the CdS film thickness in the device. Maintaining junction quality in superstrate structures with $d_{\text{CdS}} < 100$ nm depends on maintaining a uniform interface throughout the processing to avoid formation of parallel junctions between CdTe and the transparent conductive oxide (TCO).

X-ray diffraction and opto-electronic measurements of the interfacial region in high efficiency cells shows that the interface consists of $\text{CdTe}_{1-x}\text{S}_x/\text{CdS}_{1-y}\text{Te}_y$, where the interfacial values of x and y correspond to the solubility limits in the CdTe-CdS system at the device processing temperature. The $\text{CdTe}_{1-x}\text{S}_x$ and $\text{CdS}_{1-y}\text{Te}_y$ alloys form via diffusion across the interface during CdTe deposition and post-deposition treatments and affect photocurrent and junction behavior. Formation of the $\text{CdS}_{1-y}\text{Te}_y$ alloy on the S-rich side of the junction reduces the bandgap and increases absorption, reducing photocurrent in the 500 to 600 nm range [1]. Formation of the $\text{CdTe}_{1-x}\text{S}_x$ alloy on the Te-rich side of the junction reduces the absorber layer bandgap, due to the optical bowing parameter of the CdTe-CdS alloy system [2]. The increase in long wavelength spectral response increases photocurrent by ~ 0.5 mA/cm², which is nearly offset by small reduction in Voc ~ 25 mV.

Other significant effects of this alloy formation include spatially non-uniform consumption of the CdS layer, penetration of CdS into the CdTe film grain boundaries, and relaxation of

lattice strain between CdTe and CdS. Non-uniform consumption of CdS leads to parallel junctions between $\text{CdTe}_{1-x}\text{S}_x/\text{CdS}_{1-y}\text{Te}_y$ and $\text{CdTe}_{1-x}\text{S}_x/\text{ITO}$ (or SnO_2), resulting in a net increase in J_0 , which reduces Voc [3]. Penetration of S-rich species into the CdTe grain boundaries can produce a three-dimensional junction, which increases the actual junction area, also reducing Voc [4]. The grain boundary penetration of CdS in CdTe is accelerated by CdCl_2 and O_2 chemical activity during the post-deposition treatment [5] and is extremely sensitive to the physical and chemical state of the CdTe film prior to the treatment. Evidence is mounting that suggests grain boundaries play a dominant role in controlling dark diode current, photocurrent collection, and stability, and processing techniques which control grain boundary properties should aid controlling film properties over the large areas required for module manufacturing.

EXPERIMENTAL

All structures were fabricated on Corning 7059 glass. Indium-tin oxide (ITO) transparent conductive oxide (TCO) films 200 nm thick were sputtered from an $\text{In}_2\text{O}_3:\text{Sn}$ target in Ar/ O_2 ambient at room temperature. The ITO/glass structures were treated in H_2/Ar at 450°C for 15 minutes to recrystallize the films and fix the electronic properties, giving sheet resistance of 15 Ohm/sq and optical transmission exceeding 80% at 400 nm. Tin oxide films with sheet resistance of 10 Ohm/sq were deposited by APCVD at 550°C . High resistance In_2O_3 and SnO_2 transparent (HRT) buffer layers were formed by oxidation of electron beam-deposited In and Sn films on the specular ITO and SnO_2 films, respectively.

CdS films were deposited by vacuum evaporation (< 80 nm) at 220°C and chemical bath deposition (CBD) at $75\text{--}80^\circ\text{C}$. Planar chemical bath deposition (PCBD) consisted of flowing aqueous solution containing cadmium sulfate, thiourea, and ammonia onto preheated superstrates. The net deposition rate was ~ 10 nm/min and utilization of Cd species was $> 90\%$.

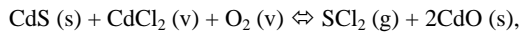
All CdS films were vapor treated in $\text{CdCl}_2:\text{Ar}:\text{O}_2$ at 400°C for 10 minutes to increase grain size and reduce formation of S-rich $\text{CdS}_y\text{Te}_{1-y}$ alloys in the CdS film. After treatment, all CdS films were overcoated with 20 nm of PCBD CdS to allow unambiguous comparison between "baseline" thickness, $d_f > 100$ nm evaporated CdS, and all-PCBD CdS films, with $d_f < 100$ nm. CdTe films were deposited by vacuum evaporation at 300 to 350°C and growth rate of 3 nm/sec at a base pressure of 2×10^{-6} Torr. Uniform CdTe films having thickness from 0.6 μm to 5.5 μm were obtained by varying deposition time. Different

post-deposition treatments were employed to control CdS diffusion into CdTe. Prior to treatment in CdCl₂:Ar:O₂ vapor, the CdTe/CdS/TCO/glass structures were annealed, either in air at 450°C, or argon at 580°C. The requisite treatment in CdCl₂:Ar:O₂ was carried out at 420°C at p(CdCl₂) from 5 to 9 mTorr and p(O₂) from 10 to 150 Torr. Contact to CdTe was obtained by vapor treatment of the CdTe surface at ~100°C to remove oxides and to produce Te excess. Cuprous telluride was formed by electron beam evaporation of copper metal followed by heat treatment at 200°C. Acheson carbon ink was used to form the current-carrying conducting back contact pad, and devices were electrically isolated by scribing through the C/Cu₂Te/CdTe.

Film morphology and structure was characterized by tapping atomic force microscopy (AFM) and symmetric x-ray diffraction (XRD). In some cases, surface phases were identified using glancing incidence x-ray diffraction (GIXRD). Optical transmission and reflection were used to determine the transmittance of oxide layers, CdS thickness, and CdTe absorption. Current-voltage and quantum efficiency-wavelength measurements were used to characterize device operation and determine final CdS thickness.

MODIFIED WINDOW LAYER RESULTS

Formation of CdS_{1-y}Te_y alloy on the S-rich side of the junction is minimized or is measurably eliminated by heat treating the CdS layer in CdCl₂:O₂:Ar vapor at 400°C prior to CdTe deposition, which increases grain size, sharpens the CdS optical transmission edge, and forms oxides, which reside on grain surfaces and penetrate grain boundaries. The oxide-producing reaction between CdCl₂ vapor and O₂ vapor and CdS is:



with free energy of reaction at 400°C of -12.5 kcal/mol. An analogous reaction occurs between CdTe in CdCl₂:O₂ ambient. Confirmation of this chemistry was obtained by detection of cadmium oxide phase in heat treated powder mixtures and films, using glancing incidence x-ray diffraction. As the stable equilibrium reaction product for the halide-air ambient, CdO is expected to behave as a barrier to subsequent reaction and diffusion of Te and Cd species from the CdTe layer into the window layer material. As an insulating oxide, CdO may also electrically passivate grain boundaries and surfaces.

Alloying CdS films with ZnS shows promise for device optimization by relaxing the thickness required to obtain a specified photocurrent. As Table 1 shows, for a specified photocurrent, e.g. ~25 mA/cm², using Cd_{1-x}Zn_xS alloy with x ~ 0.3 would enable the thickness to be increased from 25 nm to 60 nm. For fixed window film thickness, e.g. 100 nm, nearly 2 mA/cm² can be gained by using Cd_{1-x}Zn_xS alloy with x ~ 0.3 instead of pure CdS. Recent calculations showing an increase in valence band offsets in Zn-VI semiconductors suggest that addition of Zn to the interface may translate to higher Voc [6]. Devices made with 50 nm thick Cd_{0.95}Zn_{0.05}S films deposited by chemical bath deposition exhibited demonstrably higher Voc and FF than those with 50 nm or more of pure CdS with no buffer layer between the TCO and CdS (Table 2).

Table 1. Photocurrent estimates for different window layer thickness with 7059/ITO absorption and 10% panchromatic reflection loss.

d(CdS) (nm)	Photocurrent (mA/cm ²)		
	CdS	Cd _{0.7} Zn _{0.3} S	Cd _{0.5} Zn _{0.5} S
0	25.6	25.6	25.6
25	24.5	25.1	25.4
50	23.6	24.7	25.3
75	22.9	24.3	25.1
100	22.4	24.0	25.0

Table 2. AM1.5 J-V results (28°C) for devices with 7059/ITO, 7059/ITO/50nmCd_{0.95}Zn_{0.05}S, 7059/ITO/In₂O₃/CdS, and 7059/SnO₂/SnO₂/CdS window layers and evaporated CdTe. All processed with 580°C, 5 min pre-anneal and 420°C, 15 min CdCl₂:Ar:O₂ treatment.

TCO	HRT	d _f (CdS)	Voc	Jsc	FF	Eff
	nm/ type	nm	mV	mA/ cm ²	%	%
ITO	None	0	440	25.0	47	5.0
ITO	None	50	590	23.9	47	6.6
ITO	None	110	790	20.3	70	11.3
ITO	None	30 CdZnS	750	23.2	62	10.8
ITO	20 In ₂ O ₃	30	652	23.9	52	8.1
ITO	50 In ₂ O ₃	< 20	754	26.2	60	11.9
ITO	50 In ₂ O ₃	100	790	21.8	70	12.0
SnO ₂	None	0	440	18.0	46	3.5
SnO ₂	None	90	753	22.8	63	10.8
SnO ₂	50 SnO ₂	< 20	790	26.0	68	13.8

Also shown in Table 2 are results for devices fabricated with high resistance oxide buffer layers between the TCO and CdS film, demonstrating retention of junction quality for devices with CdS < 100 nm. Incorporating a high resistance SnO₂ buffer layer on SnO₂/7059 has resulted in devices with conversion efficiencies near 14% for evaporated CdTe with PCBD CdS. This beneficial interlayer may be due to improved CdS morphology since the chemical bath CdS film is conformal to the larger grain size obtained with oxidized metal films. Figure 1 shows AFM images of the surface morphology of as-deposited conventional CBD CdS films on ITO/7059 and PCBD CdS films on ITO/7059 and In₂O₃/ITO/7059 substrates. The CBD film contains numerous adherent particulates of homogeneously nucleated CdS and other CBD bath reaction products. In contrast, the PCBD films are free of debris and are conformal to the In₂O₃ surface. Similar results were obtained with SnO₂ HRT superstrates.

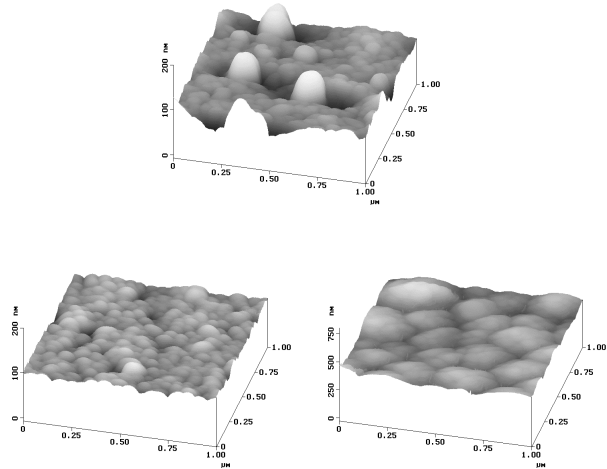


Figure 1. Tapping atomic force microscope images of CBD (top) and PCBD (lower, left and right) CdS films. The CBD and left PCBD films are on specular ITO/7059 glass. The right PCBD film is on $\text{In}_2\text{O}_3/\text{ITO}/7059$.

CDTE AND TREATMENT RESULTS

$\text{CdTe}_{1-x}\text{S}_x$ alloys in the absorber layer can have both beneficial and deleterious effects on device operation depending on how the alloys are formed, their composition and their compositional distribution. When the alloys form solely by diffusion of S and Cd species from the CdS film during $\text{CdCl}_2:\text{O}_2:\text{Ar}$ vapor treatment, S concentration will be greatest at the interface and along grain boundaries, and the CdS film may be non-uniformly consumed [7]. In this case, CdS consumption can be limited by reducing grain boundary diffusion, CdCl_2 and O_2 vapor concentrations and treatment temperature. A viable processing route already established for minimizing CdS consumption is utilizing uniform $\text{CdTe}_{1-x}\text{S}_x$ alloy absorber layers in place of pure CdTe [8].

However, with pure CdTe absorber layers, minimizing grain boundary diffusion can be accomplished by either depositing large grain CdTe films or by modifying small-grain CdTe films prior to the $\text{CdCl}_2:\text{O}_2:\text{Ar}$ vapor treatment. Typically, large-grain CdTe films are deposited at high temperature, from 400°C to 600°C . Small-grain CdTe films can be modified by a high temperature anneal at 550°C to 650°C to recrystallize the film [9] or by a moderate-temperature treatment at 400°C to 450°C in oxygen-containing atmosphere to form penetrating native oxides in the CdTe film. These oxides, detected using GIXRD, consist primarily of CdTeO_3 , are relatively stable during subsequent $\text{CdCl}_2:\text{O}_2:\text{Ar}$ vapor treatment and retard grain boundary diffusion of CdS as seen by the near elimination of the $\text{CdTe}_{1-x}\text{S}_x$ alloy tail in x-ray diffraction line profiles. During CdCl_2 treatment, CdO is also formed as a result of chemical interaction between the CdTe and the treatment ambient. Controlling the degree of oxide formation and interdiffusion with thin CdTe layers depends on optimizing the pre-anneal steps, the vapor composition and reaction temperature used during the CdCl_2 treatment.

Figure 2 compares the $\text{CdTe}_{1-x}\text{S}_x$ XRD (511/333) line profiles after treatment in $\text{CdCl}_2:\text{O}_2:\text{Ar}$ vapor for different pre-treatments of 1.3 micron thick CdTe/CdS. The line profiles have been normalized to the same area and contain quantitative information of the S content and distribution in the absorber layer. In the upper figure, a sample with argon pre-anneal at 580°C for 5 minutes exhibits significantly less $\text{CdTe}_{1-x}\text{S}_x$ alloy, hence CdS consumption, than the sample with no pre-anneal; the pre-annealed sample contains an equivalent CdS thickness of 13 nm, compared to 53 nm for the non-annealed sample. In the lower figure, 450°C air pre-anneal is shown to retard CdS diffusion, resulting in equivalent CdS consumption of 45 nm for 10 minutes and 35 nm for 20 minute pre-anneal treatment. For the CdCl_2 treatment temperature used, at $T = 420^\circ\text{C}$, the limiting $\text{CdTe}_{1-x}\text{S}_x$ alloy composition is given by the empirical expression,

$$x = -0.0149 + (1.207 \times 10^{-4})T + (3.940 \times 10^{-8})T^2 + (2.393 \times 10^{-10})T^3$$

for T in Celsius and occurs at $x = 0.06$, corresponding to $2\theta = 76.83^\circ$ from,

$$2\theta = 2 \sin^{-1} \frac{1.508}{2 \sqrt{h^2 + k^2 + l^2} (9.7734 - x)}$$

where x is the alloy composition, 2θ is the diffracting x-ray wavelength and h,k and l are the Miller indices of the diffracting plane.

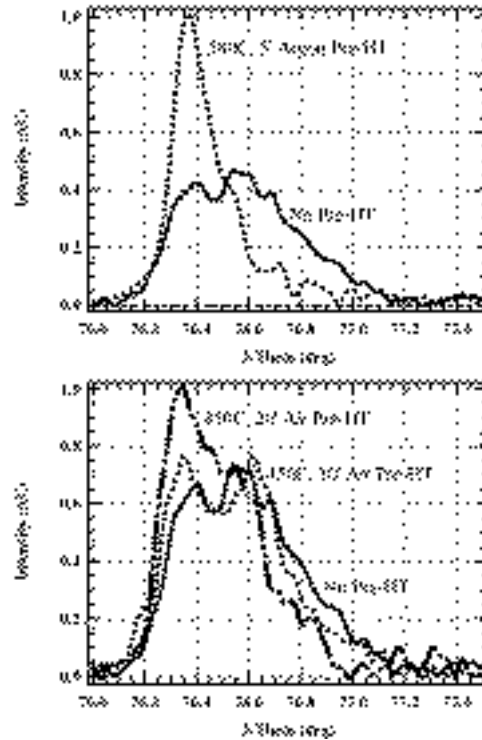


Figure 2. X-ray diffraction line profiles of $\text{CdTe}_{1-x}\text{S}_x$ (511/333) of CdTe/CdS films treated at 420°C in $\text{CdCl}_2:\text{O}_2:\text{Ar}$ vapor with and without pre-anneal (pre-HT) step. Top: argon pre-HT; Bottom: air pre-HT.

These processing techniques enable devices with thin CdTe layers to be optimized with thin CdS window layers. The measured absorption in PVD CdTe samples reveals that photocurrents greater than 27 mA/cm² are possible with AM 1.5 spectral illumination for d(CdTe) > 0.6 microns. The beneficial effect of pre-anneal treatment on devices with 4 micron and 1 micron thick CdTe absorber layers are shown in Table 3. For these samples, the CdTe films were deposited at 340°C, and the same CdCl₂ treatment used for the samples of Figure 2 was performed, at 420°C. For both sample sets, the pre-anneal treatment improved junction quality compared to no pre-anneal. In the devices, the low fill factors are primarily due to low diode quality factor and high series resistance. For the samples with 1 micron thick CdTe, the fill factor is additionally affected by shunting, which may be due to non-optimized contact processing. Nevertheless, the current collection in these devices is unaffected by the CdTe thickness and is indistinguishable from devices with thicker CdTe, demonstrating the potential for further optimization of CdTe devices with thin CdTe.

Table 3. AM1.5 J-V results (28°C) for devices with thin CdTe deposited at 340°C on 7059/ITO/CdS.

d CdTe	Pre- Anneal	d _f CdS	Voc	Jsc	FF	Eff
μm		nm	mV	mA/ cm ²	%	%
4.0	None	100	700	22.0	55	8.5
4.0	Air	120	735	21.0	65	9.2
4.0	450°C, 20 min Argon	100	785	23.0	63	11.3
	580°C, 5 min					
1.3	None	100	664	22.5	47	7.0
1.3	Air	150	722	20.0	57	9.4
	450°C, 20 min					
1.3	Argon	100	766	22.4	55	9.3
	580°C, 5 min					

SUMMARY

Resistive In₂O₃ and SnO₂ films formed by oxidizing metal films allow junction quality to be maintained for devices with d(CdS) < 100 nm. Conformal CdS films deposited by PCBD have high Cd utilization and have low pinhole and particulate occurrence, contributing to process robustness. PCBD Cd_{1-x}Zn_xS films may be used *in lieu* of CdS/HRT to retain junction quality while obtaining high J_L. Continuous, dense PVD CdTe films with d(CdTe) from 4 microns to 1 micron deposited at T < 400°C can be optimized by use of a pre-anneal step and vapor CdCl₂ treatment to control oxide formation and interdiffusion. Devices made with d(CdTe) ~ 1 micron show promise for development of cells with CdTe thickness near the optical limit for absorption.

ACKNOWLEDGEMENTS

This work was supported by the United States Department of Energy through the National Renewable Energy Laboratory and the support of the New Energy and Industrial Technology Development Organization (NEDO). Specular tin-oxide coatings on Corning 7059 glass were provided by Anthony Catalano. The contributions of Shannon Fields, Greg Hanket, Kevin Hart, Steven Hegedus, Jie Zhu, Wayne Buchanan, Chuck Debo and Paula Newton in carrying out this research are gratefully acknowledged.

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