Parallelism IV

John Cavazos

Dept of Computer & Information Sciences

University of Delaware

Lecture Overview

- Profiling
  - Intel® ISAT
  - Intel® Vtune™ Amplifier XE Evolution

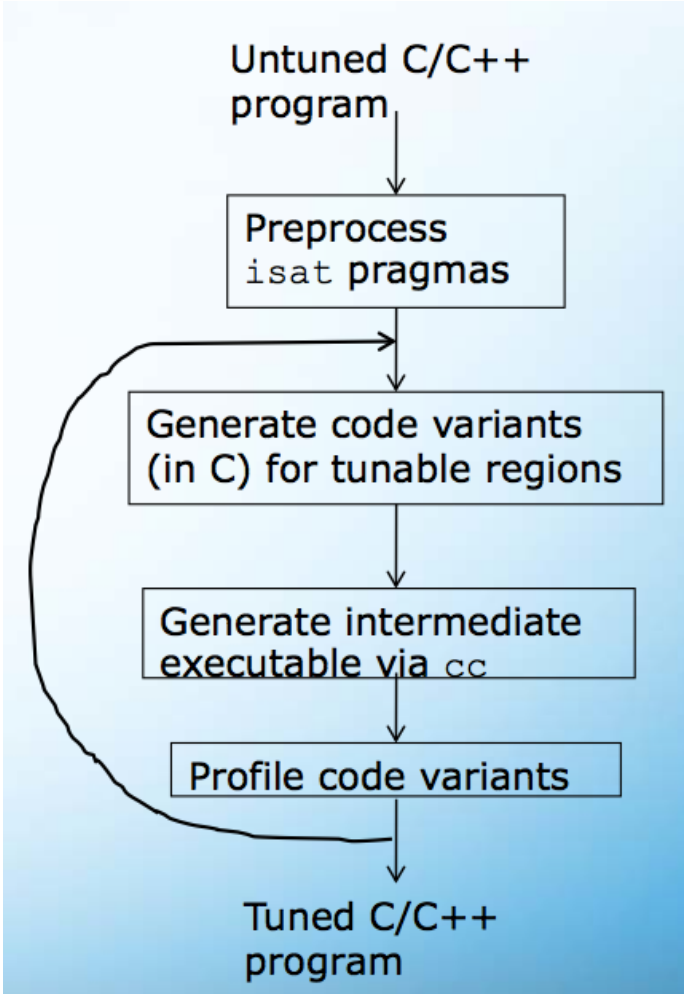
ISAT

- Intel® Software Autotuning Tool (ISAT)
  - http://software.intel.com/en-us/articles/intel-software-autotuning-tool/
  - Supports automatic search of the near-optimal values of important program parameters
    - Examples: OpenMP, Intel TBB (Threading Building Blocks)
  - Visualizes tuning results
  - Identifies regions that need tuning
  - Compiler independent

source: http://www.ckluk.org/ck/talks/cilkplus-tutorial-ppopp11.pdf

Quick Overview of ISAT

- Implemented in Python
  - Source-to-source translation
- Work with any C/C++ compilers
- Thread-safe implementation



source: http://www.ckluk.org/ck/talks/cilkplus-tutorial-ppopp11.pdf

Example: OpenMP

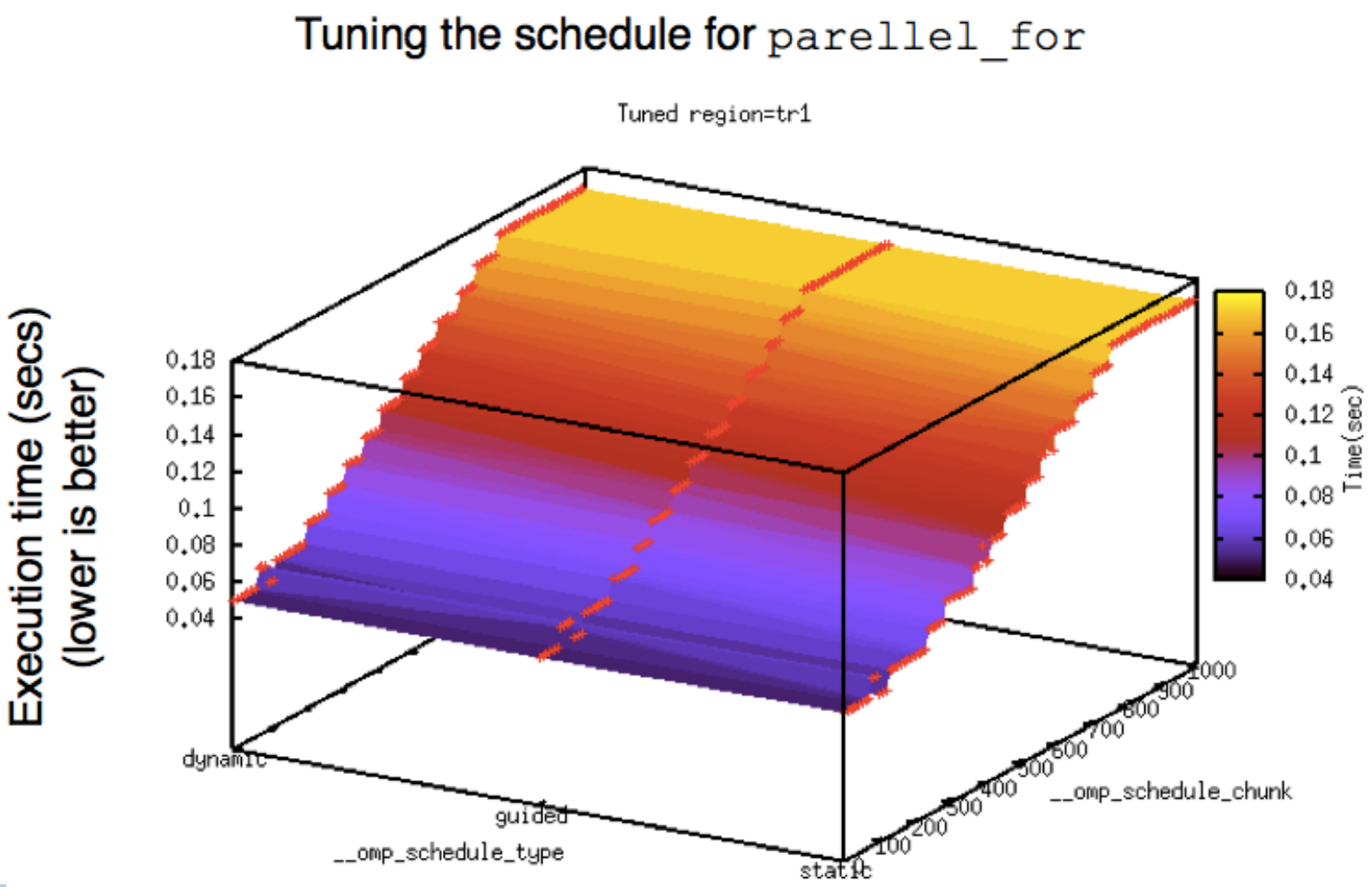
```
#pragma isat tuning
variable(@omp_schedule_type, [static, dynamic, guided])
variable(@omp_schedule_chunk, range(0, 1000, 100))
search(dependent)

#pragma omp parallel for
for(i = 0; i < N; i++)
    C[i] = A[i] * B[i];
```

- ISAT supports the tuning of the scheduling parameters in OpenMP loops (`parallel for` and `parallel do`)
- Two tunable parameters: schedule type and chunk size
- Specification of values
  - Explicit list using [ ] or range(begin, end, stride)
- Search scheme: dependent or independent

source: http://www.ckluk.org/ck/talks/cilkplus-tutorial-ppopp11.pdf

Visualization of Result



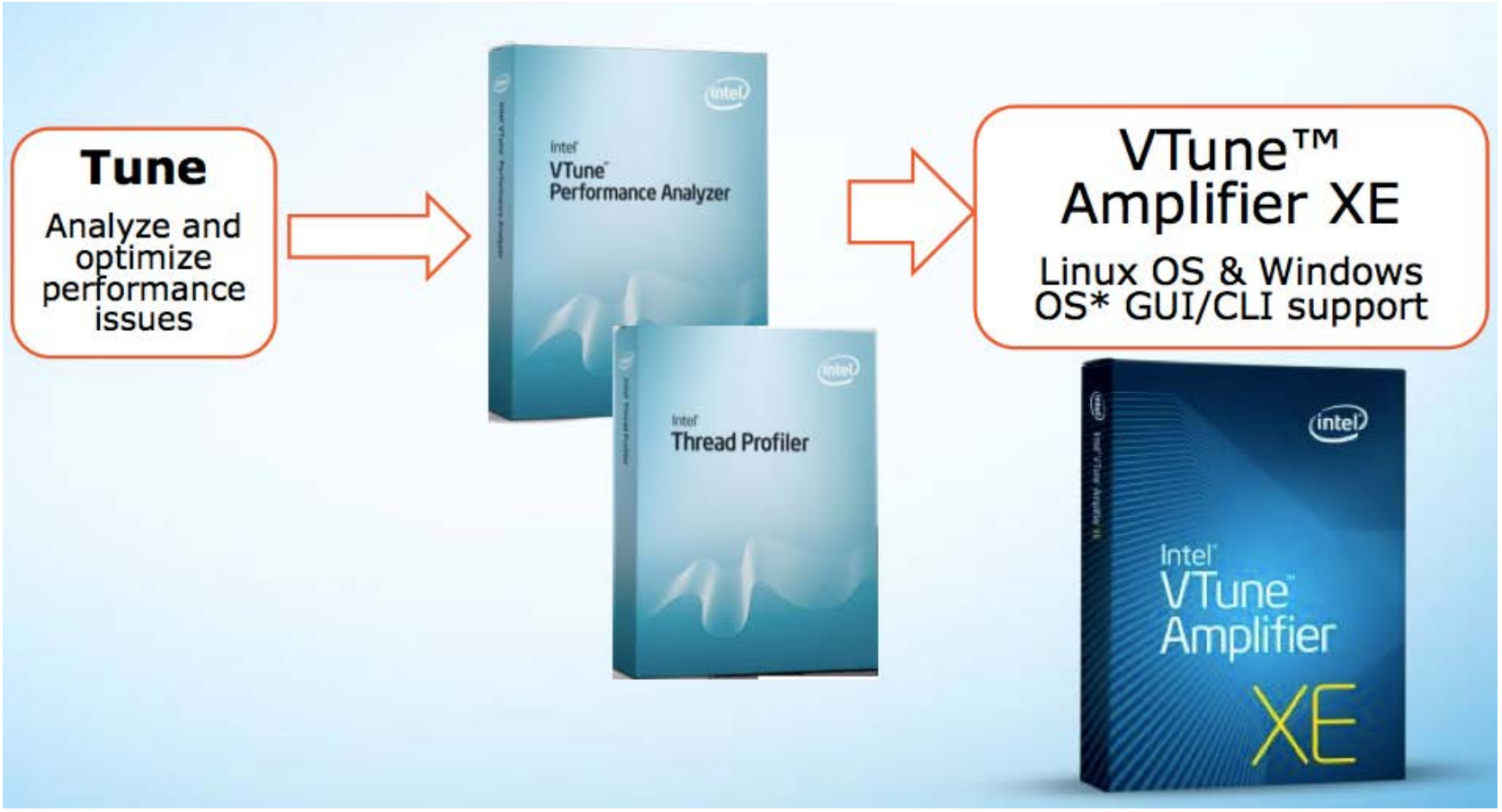
source: http://www.ckluk.org/ck/talks/cilkplus-tutorial-ppopp11.pdf

Future work for ISAT

- Support for tuning MPI programs
- Tune for Energy
  - Feasible on SandyBridge with its energy counters
- Advanced search strategies
  - Machine learning
- Search for the best permutations of compiler optimizations

source: http://www.ckluk.org/ck/talks/cilkplus-tutorial-ppopp11.pdf

Vtune™



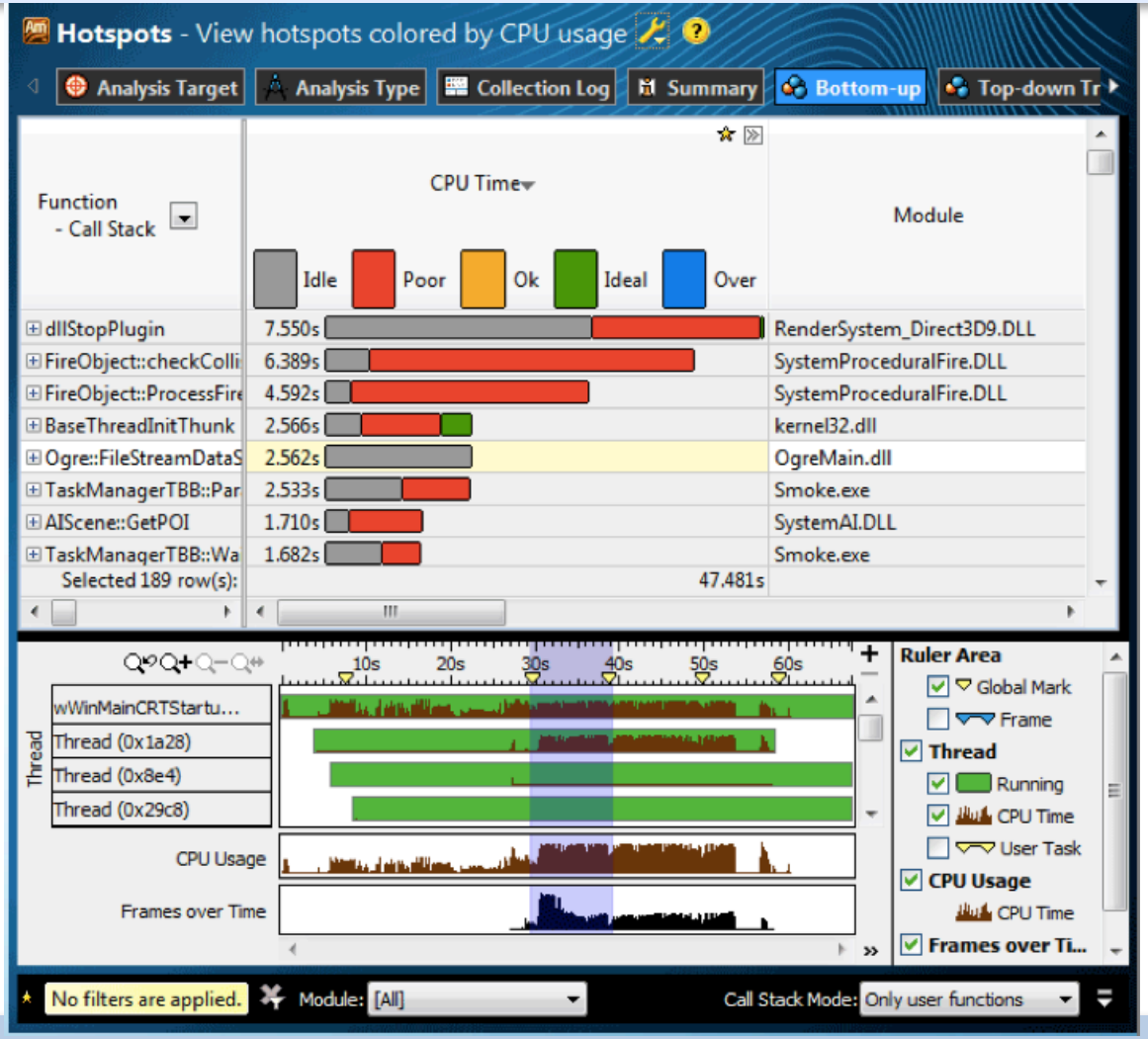
source: http://tools.zih.tu-dresden.de/2011/downloads/Intel_Using_VTuneAmplifierXE_for_HighPerformanceComputing_r0.9.pdf

Quick Overview of VTune™

- Performance Profiles
  - Hotspot
  - Hardware-Event Based Sampling (EBS)
- Locks and waits analysis
- Thread Profiling
  - Visualize thread interactions on timeline
  - Balance workloads
- Hardware event sampling

source: http://tools.zih.tu-dresden.de/2011/downloads/Intel_Using_VTuneAmplifierXE_for_HighPerformanceComputing_r0.9.pdf

Example: Hotspot Analysis



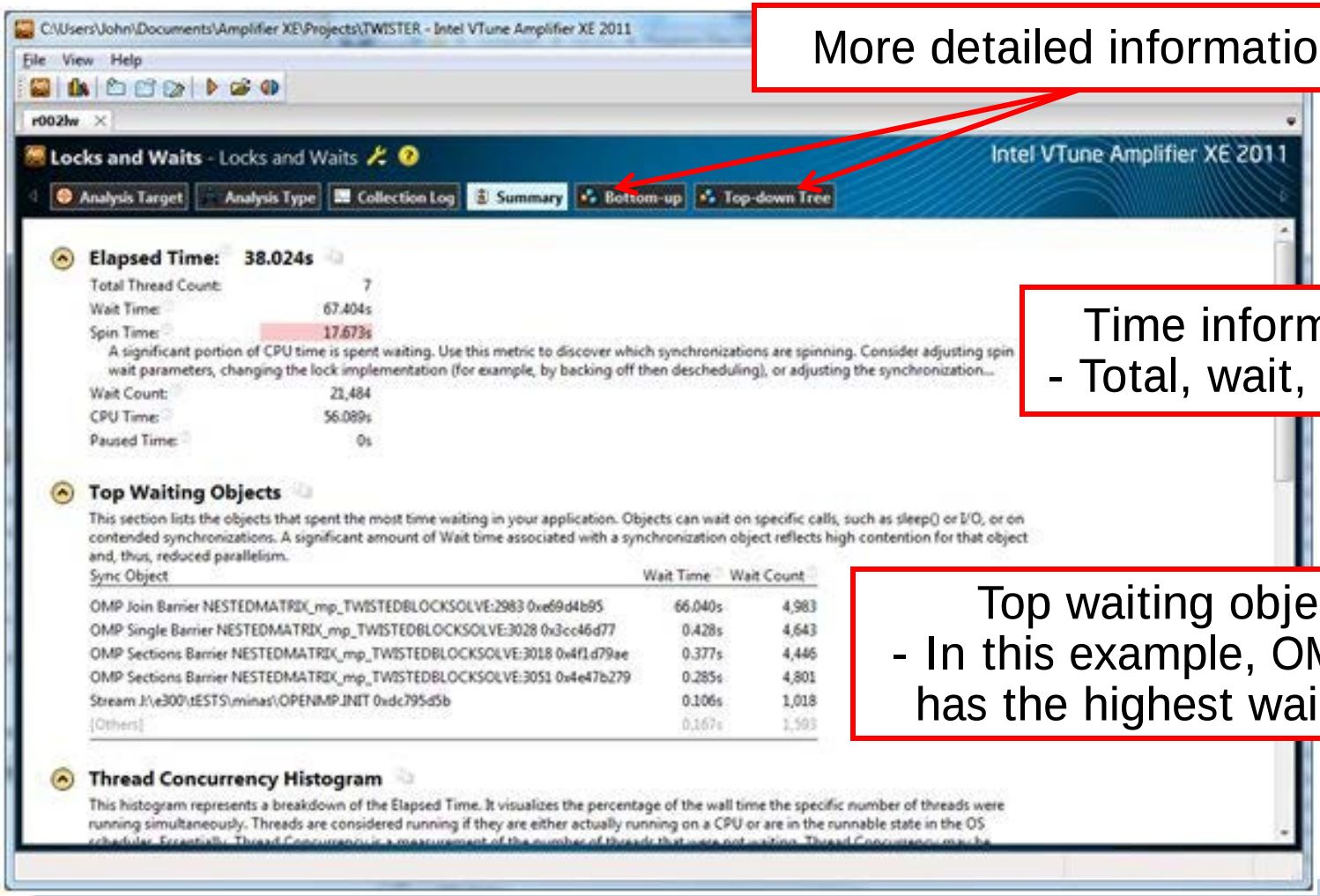
source: http://tools.zih.tu-dresden.de/2011/downloads/Intel_Using_VTuneAmplifierXE_for_HighPerformanceComputing_r0.9.pdf

Example: OpenMP Analysis

- Identifies where your application is waiting on synchronization objects or I/O operations
- Discovers how these waits effect your application performance

source: http://www.polyhedron.com/plain-VTune

Example: OpenMP Analysis



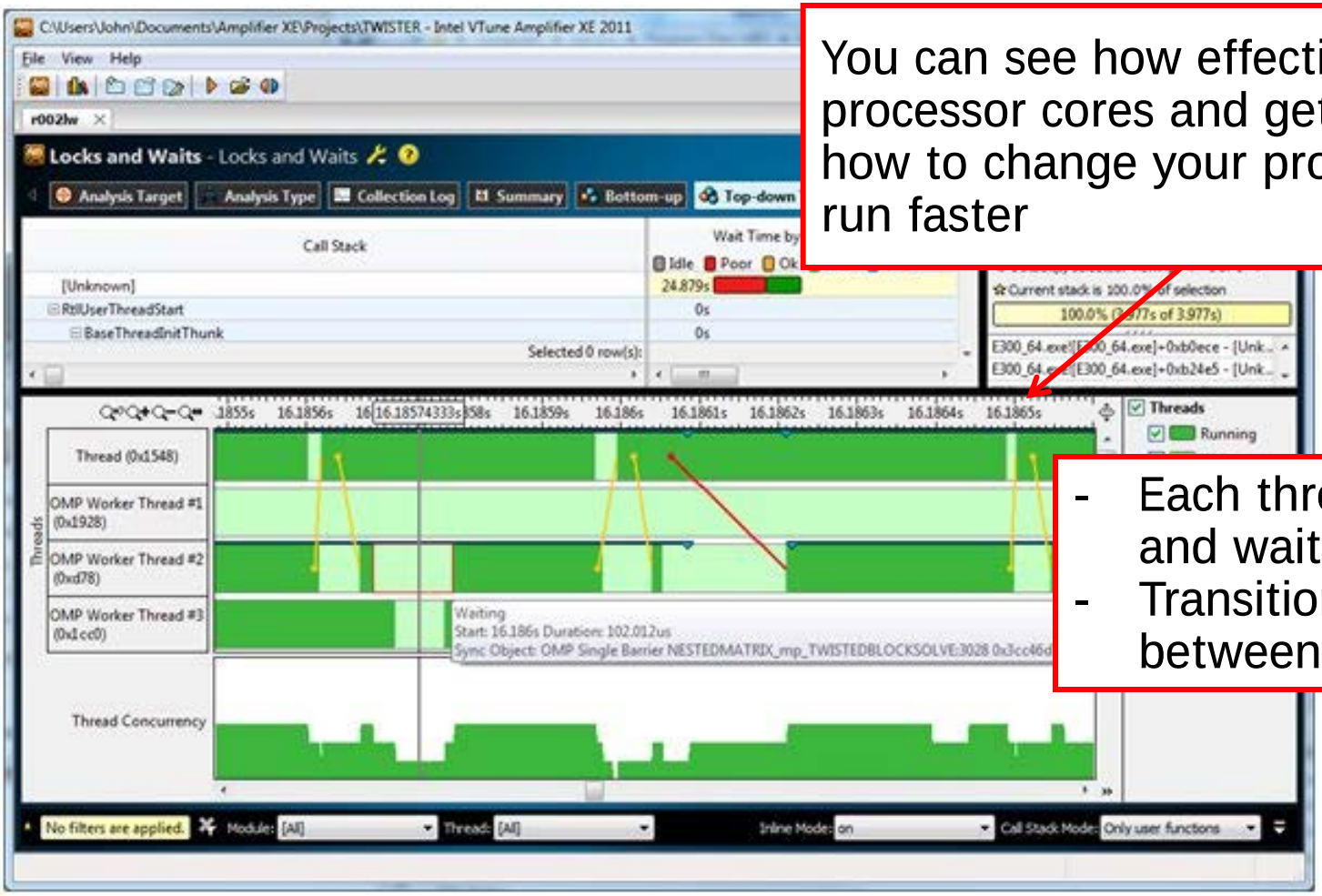
More detailed information

Time information
- Total, wait, spin, ...

Top waiting objects
- In this example, OMP Join has the highest wait time

source: http://www.polyhedron.com/plain-VTune

Example: OpenMP Analysis



You can see how effectively using processor cores and get insights how to change your programs to run faster

- Each thread's run and wait
- Transitions between threads

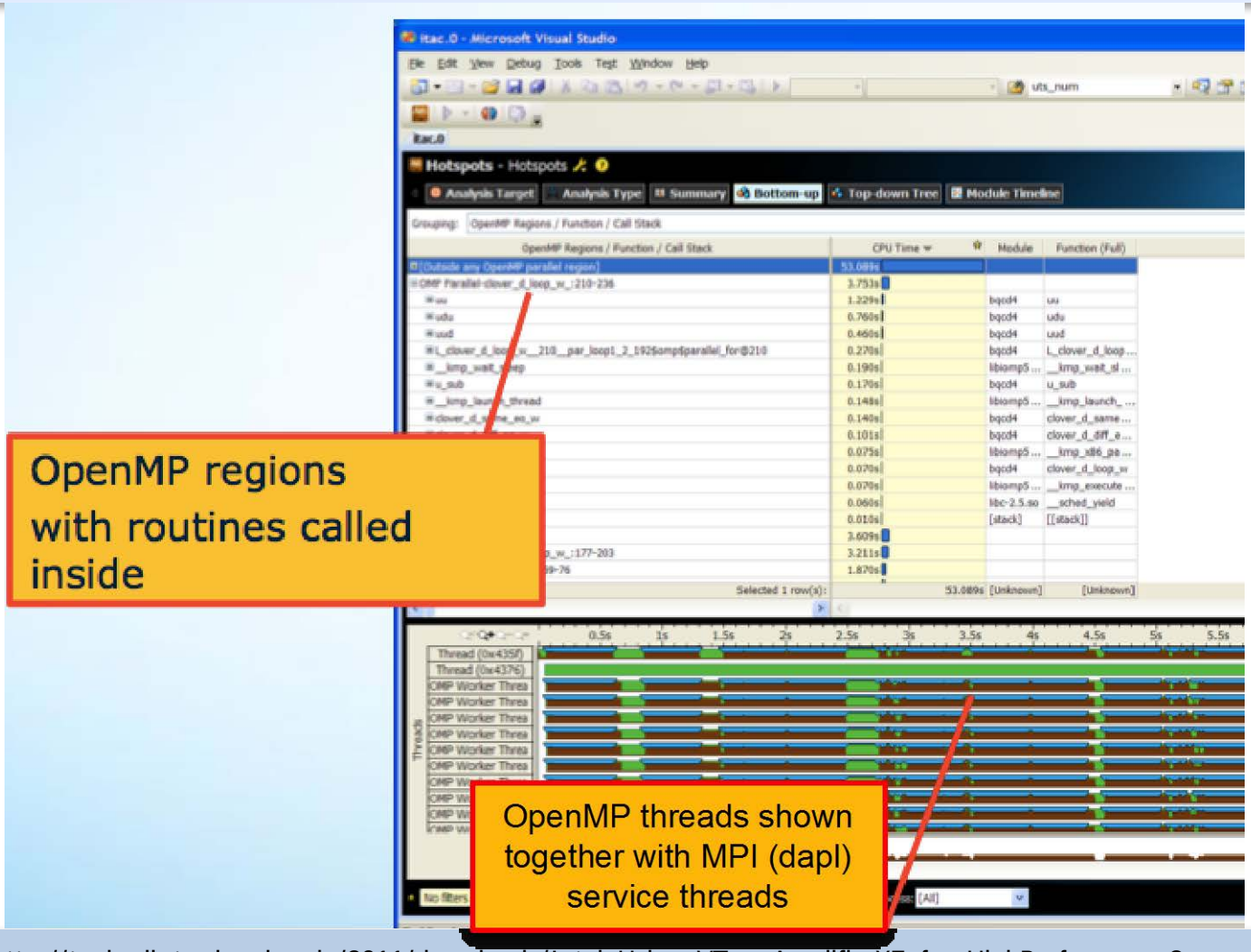
source: http://www.polyhedron.com/plain-VTune

Example: MPI Analysis

- Use `amplex-cl` command to collect data and post-process results
  - Individual result directory will be created for each spawned process
- Example
  - `> mpiexec -n 4 amplex-cl -r my_result -collect hotspot -- my_app [my_app options]`
  - This will create result directory for 4 processes named my_result.1 to my_result.4
- Using GUI viewer to analyze each result

source: http://www.polyhedron.com/plain-VTune

Example: MPI Analysis



source: http://tools.zih.tu-dresden.de/2011/downloads/Intel_Using_VTuneAmplifierXE_for_HighPerformanceComputing_r0.9.pdf

Future Work for Vtune™

- Upcoming updates
  - Will be part of Intel® Cluster Studio XE
  - Will be supported on clusters

source: http://tools.zih.tu-dresden.de/2011/downloads/Intel_Using_VTuneAmplifierXE_for_HighPerformanceComputing_r0.9.pdf

Performance Counters

- Special purpose registers built into the processor microarchitecture
  - Monitor hardware-related activity within the computer
- Useful for performance analysis and tuning
  - Provide low-level information that can not be obtained with software profilers

source: http://pcsostres.ac.upc.edu/eitm/lib/exe/fetch.php/slides:pmc.pdf

Performance Counters

- Example of Events
  - Cache Line Access
  - Cache Access in Different Level (1,2, and 3)
  - Branch Prediction Related Events
  - Number of Total Cycles and Instructions
  - Number of Interrupt and Stall Cycles
  - …