

Workshop from the Thin Film Photovoltaic Symposium: Semiconductor Processing and Manufacturing

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SUMMARY

The viability of semiconductor deposition and treatment processes for manufacturing are assessed and critical issues identified for CdTe, Cu(InGa)Se₂, thin film silicon, and amorphous silicon technologies. The focus is on increasing throughput and decreasing costs. Specific issues include deposition rate, materials utilization, adhesion, uniformity, equipment and process scale-up, compatibility with subsequent processing, module performance, and environmental concerns.

INTRODUCTION

The objective of the Workshop on Semiconductor Processing and Manufacturing was to examine criteria by which semiconductor deposition and treatment processes can be assessed and selected for improved manufacturability. This is critical to allow the intelligent transfer from laboratory scale processing to commercial scale manufacturing. The concept of improved manufacturability can be simply defined as reduced module costs, i.e., dollars per watt, and increased process throughput and yield, i.e., watts per fabrication time. The semiconductor deposition and processing are typically the most expensive steps in the manufacture of thin film photovoltaic modules.

The workshop was held at the Thin Film Photovoltaic Symposium at the University of Delaware on May 1, 1997. The workshop panel included its organizer William Shafarman of the Institute of Energy Conversion (IEC), Bulent Basol of International Solar Electric Technology (ISET), Jeff Britt of Energy Photovoltaics (EPV), Robert Hall of AstroPower, and Richard Rocheleau of the Hawaii Natural Energy Institute of the University of Hawaii. The workshop began with an introduction by William Shafarman to the concepts which the panelists agreed were

generically important. Subsequent presentations by the panel were organized by different material systems. Jeff Britt discussed several issues critical to the scale-up of Cu(InGa)Se₂ technology, including adhesion, uniformity, and growth rate. Bulent Basol discussed the need for a methodology to assess thin film processing as applied to CdTe and the specific need to control interaction between the CdS and CdTe layers. Rick Rocheleau addressed critical issues for amorphous Si manufacturing, focusing on increasing throughput with greater a-Si growth rate. Finally, Bob Hall talked about crystalline Si grown on a low cost substrate with the example of an improved process for emitter formation. These presentations were followed by open discussion in which some of these issues were discussed further and several additional issues were raised. In this workshop report the main points made by each panel member will be reported. Then, some of the main points of the open discussion will be summarized, but without identifying the audience members.

MANUFACTURABILITY ISSUES

Issues to reduce thin film semiconductor process costs and increase throughput can be categorized as either technical issues which should be addressed, in part, at the laboratory scale, or as scale-up issues which must apply to a specific process. The technical issue which receives the most attention is device efficiency. High device and module efficiency obviously can reduce module cost when measured as cost per watt of output. Other technical issues which must be demonstrated for a particular process include structural issues like compositional and morphological tolerances and good adhesion. The compatibility of the semiconductor deposition or processing with the overall device and other process steps should also be demonstrated at the laboratory scale. For example, the film surfaces must be compatible with simple contacting or junction formation processes. The process

temperature is typically restricted by the type of substrate or previously deposited layers. Modifying the bandgap of the absorber layer can improve module performance and reduce constraints on transparent conducting oxide layers and interconnects.

Materials costs can be reduced with the use of lower cost source materials, particularly if the use of hazardous materials can be eliminated. There is also a need to develop processes with greater materials utilization and reduced film thicknesses. Uniformity of composition, electrical and optical properties, as well as materials utilization, must be addressed in a large scale process but the tolerances to these parameters should be determined at the laboratory scale .

A manufacturing facility designed to produce 10 MW of PV in a year with 40 W modules needs to produce approximately 1 module per minute. A process can be made compatible with this high throughput by reducing the deposition time and incorporating the deposition and other steps in an in-line sequence. Alternatively, for longer deposition times, parallel or batch processing can be used but with higher capital costs. The effect of increased growth rate on device fabrication and performance should be a primary focus of laboratory scale research. Throughput can also be increased with thinner layers and simpler processes since additional layers or controlled compositional or dopant grading can increase deposition time.

CdTe PROCESSING

Many options for depositing CdTe thin films for PV have been demonstrated^{1,2} so the question posed was which criteria need to be addressed in choosing the best deposition process for scaling up to large area and high rate manufacturing. There is a lack of sufficient understanding to determine whether a CdTe film is suitable for high device or module performance without fabricating and characterizing those

devices, so evaluating different deposition processes is more complicated. To assess processing options for CdTe it is necessary to first understand the material and determine the critical properties needed in the thin film and other parts of the device structure. The next step is to understand the deposition and processing techniques and determine if they have the capability of providing the critical properties needed in the various layers without apparent limitations. Finally, the reproducibility and uniformity must be assessed and means for process control developed.

CdTe processing generally includes three steps; deposition, post-deposition treatment, which typically incorporates cadmium chloride, and contacting. Different deposition options for CdTe include closed space vapor transport, electrodeposition, thermal evaporation, screen printing, and sputtering. In all cases, sufficient deposition rates have been demonstrated so that, at least in batch mode, large throughput is feasible. The post-deposition treatments have been developed so that, along with the deposition, films can be reproducibly produced with columnar grain structure and good control of stoichiometry. Good device or module performance requires a CdS layer thin enough to minimize optical absorption. A critical problem is the CdS/CdTe interaction which occurs during deposition and especially during post-deposition treatment which directly affects the device performance.³ There is a need to either modify the device structure to compensate for the interdiffusion, e.g., by eliminating the CdS layer entirely, or to control the interdiffusion. Different deposition methods give films with vastly different structure including grain size and porosity. Therefore, control of the CdS/CdTe interdiffusion will depend on the specific deposition method used.

While different processes generally incorporate oxygen, it is not known what its role is and if it primarily affects the bulk CdTe or surfaces and grain boundaries. Again, the oxygen incorporation needs to be understood and controlled and this is

expected to depend on the structure of the films and therefore on the process for CdTe deposition.

Cu(InGa)Se₂ ISSUES

Several major issues confronting the manufacture of Cu(InGa)Se₂ modules were raised including adhesion of the Cu(InGa)Se₂, composition control, and throughput. These issues were discussed particularly with regard to processes using sequential deposition of metallic or binary precursor films and selenization to form the Cu(InGa)Se₂. While these processes are being pursued by several industrial groups, most non-industrial, laboratory scale research is focused on multisource elemental evaporation to deposit the Cu(InGa)Se₂. Adhesion failure at the Mo/Cu(InGa)Se₂ has been widely observed with selenized films but is not considered a significant problem with multisource evaporation. The adhesion failure was attributed to stress in the film plane and lack of intimate contact between the Mo and Cu(InGa)Se₂ layers. Selenization is being pursued by several groups who have shown improved adhesion with the addition of interfacial layers such as Ga,⁴ Te,⁵ or GaSe.⁶ However, it is unknown whether these interfacial layers relieve stress and have better adhesion to the Mo or reduce voids at the interface.

One of the remarkable properties of Cu(InGa)Se₂ is the wide range of composition that can be tolerated, with good device performance demonstrated for $0.8 < \text{Cu}/(\text{In}+\text{Ga}) < 1.0$. Still the composition both parallel and normal to the film surface must be controlled. While several deposition methods can provide uniform deposition, sequential processes like selenization may be preferable because the uniformity of individual metal layers is simpler to monitor than the simultaneous delivery and reaction of all species. Composition control requires simple

monitoring and there is a need for methods to determine the composition quickly and non-destructively, which can be incorporated directly in-line, if possible.

Different deposition methods for Cu(InGa)Se_2 present varying opportunities to increase throughput by increasing deposition rate or reaction time. For example, Figure 1 shows the efficiency of devices made at EPV on Cu(InGa)Se_2 films formed by the selenization of precursor films⁷ with the total Se exposure time varied from 4.5 to 33 minutes, excluding heat-up or cool-down times. In this case there was only a decrease in device efficiency from 12.4% at the longest time to 10.5% for the shortest time. Reaction rates for the formation of Cu(InGa)Se_2 ⁸ are needed to determine the maximum throughput and whether limits to deposition rate are fundamental or process specific.

THIN FILM Si

The criteria for assessing the manufacturability of a specific process were discussed and applied specifically to the comparison of two different processes for emitter formation on polycrystalline silicon grown on a low cost substrate at AstroPower. After a specific process and product design have been determined and the product performance and stability demonstrated, the costs can be evaluated and minimized. In this case, a batch process for emitter formation performed in a quartz tube, similar to processes used in other semiconductor manufacturing, was being used. An alternative process for continuous emitter layer formation on a moving belt was proposed and the process demonstrated on a laboratory scale.

A comparison of the criteria used to assess these two processes is given in Table I. For the batch process, the material costs were high due to the use of expensive and hazardous gases. Capital equipment costs were relatively low because equipment was readily available. Operating costs include electricity and

consumables, which in this case were high because quartz carriers and tubes break periodically. Labor costs were also high because samples were manually loaded and transferred. Process yield is a critical parameter and was high in this instance. But equipment utilization was low because the batch process means that the long heat-up and cool-down times consumed 50% of the equipment operation time.

The continuous process did not require the carrier gases so material costs are lower. This was not an established process, so capital investment in this case depended on whether equipment was built in-house or purchased. Usually, it is preferable for equipment to be purchased from an experienced equipment manufacturer. Operating costs were lower since there were fewer consumable components, and labor costs were also lower since there was less manual handling. Process yield could be improved because the planar geometry was more favorable for thermal energy transfer. Finally, the equipment is utilized much more efficiently in the continuous mode.

Table I. Comparison of costs associated with batch and continuous processes for emitter formation on thin film silicon.

Cost	Batch - Tube	Continuous - Belt
process demonstration	yes	yes
material cost	high	lower
capital investment	low	higher
operating cost (excl. labor)	costly carriers	lower, no carriers
labor cost	high - manual transfer	lower - mechanized
process yield	> 90%	> 90%
equipment utilization	50%	> 90%

Maintaining low costs for a process in a manufacturing environment depends on the process dependability, repeatability, and maintainability. Dependability depends on minimizing the mean time between failures which requires equipment which has been “hardened” for manufacturing. Repeatability requires a process with no

variation, while maintainability depends on the utilization of well documented procedures.

a-Si ISSUES

Plasma processes for amorphous silicon deposition on a commercial scale are more advanced than other thin film PV technologies. Essential issues like adhesion, uniformity, and compatibility with subsequent or previous processing have been demonstrated on a pilot scale with a variety of module and reactor designs. Examples of different processes and design choices which are being evaluated on the pilot scale include dc or rf plasma, substrate or superstrate configurations, batch or continuous processing, and single, tandem, or triple junction devices. The overall cost per watt of output can be expressed simply as the direct costs divided by the capacity, and for a-Si the semiconductor deposition is the most expensive step. The direct costs include the capital costs of the reactor as well as peripherals such as pumping and gas handling systems plus the variable costs including materials, labor, and utilities. The capacity is proportional to the throughput, the efficiency, and the yield.

Some critical needs for a-Si processing were identified. First, there is the need to recognize that commercial scale equipment is fundamentally different than laboratory equipment and requires a higher level of understanding. The complexity and size of the commercial scale deposition equipment limit its flexibility and the ability to diagnose problems; therefore, there should be increased emphasis on process modeling so equipment can be designed correctly from the beginning.

The issues that drive cost need to be given as much priority in laboratory scale experiments as the issues that drive efficiency. Specifically for a-Si, high throughput devices and processes must be developed by increasing growth rates and

equipment yield. Deposition rates used by manufacturers are typically $\sim 3 \text{ \AA}/\text{sec}$. Efforts with higher rates have generally resulted in decreased device performance⁹, but there are no fundamental reasons known why rates cannot be significantly increased. Similar emphasis should be placed on increasing materials utilization. Ten percent utilization of process gases is typical. While silane is relatively inexpensive, germane used to make SiGe layers in multijunction devices is more expensive. The growth chemistry will change with higher rates so it must be understood fundamentally. Amorphous silicon manufacturing costs can also be minimized by simplifying device designs. For example, increasing the number of junctions or adding buffer layers between device layers or junction may improve device performance but will also increase the cost. So increased emphasis on maintaining good device performance with higher rate, higher utilization, and simpler processes can directly benefit a-Si manufacturing.

Finally, as with all thin film materials, there is a need for on-line diagnostics to improve control of material properties and also a need to develop quantitative understanding of process tolerances.

DISCUSSION

One approach to increase the throughput of PV module manufacturing is the use of batch or parallel processes instead of in-line processes. Manufacturing equipment for a batch process with multiple parallel process chambers will be expensive to fabricate and maintain. However, down-time can be reduced by the ability to service one process chamber while others are kept on-line. With a completely in-line process, a long deposition or process step will require an excessively long process chamber to maintain a sufficient throughput and this is expensive to manufacture and maintain. However, high deposition rates cannot be reliably achieved by merely

increasing the delivery of species to the substrate with higher source temperatures, powers, or increased gas flow rates. Most processes lack the complete understanding of growth chemistry and reaction kinetics necessary to achieve high rates and to design large scale equipment to scale up these high rate processes.

There was considerable discussion about what should be the priorities of supported laboratory scale materials and device research. Several workshop attendees agreed with the panel speakers that university research and laboratory scale experiments should focus more directly on process issues directly related to scale-up. This includes focusing on the specific processes being developed by the industrial groups. Too great a focus on achieving record efficiencies on small area devices raises the danger of developing processes that are irrelevant to manufacturing. A simple example is the effort spent on optimizing anti-reflection layers and grids for small area devices which will not be scaled up for manufacturing. If industry requires high rate processes and improved materials utilization, then laboratory scale research should focus first on developing high rate processes with greater materials efficiency, and then try to improve the resulting device efficiency. Similarly, since low cost manufacturing requires low cost substrates, there is little benefit to developing processes which use a high cost substrate.

On the other hand, focusing on achieving new high efficiencies also has potential benefits. This can be the means to develop new, fundamental understanding that leads to breakthroughs and the next generation of thin film devices and modules. At the very least, it was argued, efficiency is a grade to evaluate the processes being employed. Also, efficiency is still the most useful quantitative means for assessing different processes. If the ultimate goal is to reduce the cost per power output, then efficiency is as important as any other

parameter. For example reducing the area needed to yield a given output reduces the relative cost of the substrate.

Reducing high process temperatures for the polycrystalline materials CdTe and Cu(InGa)Se₂ was also identified as a means to reducing costs. High temperatures in a batch mode require long heat-up and cool-down times, which reduce equipment utilization and throughput, and the thermal load on deposition and process systems increases costs and potential down-time.

The workshop was reminded to keep safety issues in mind, in part because improved safety can be another means by which costs can be reduced. A specific example pertained to the use of hazardous gases such as those used in a-Si deposition or hydrogen selenide used for some Cu(InGa)Se₂ processes. Reducing gas flow rates or using more dilute gases not only lowers material costs but translates to less frequent cylinder changes and therefore lower chance of incidents which are most likely during those changes.

Finally, after extensive discussions about costs, the question was posed whether the only reason that we don't have thin film modules on the market with 12-15% efficiency is that not enough money has been invested or if there is still a fundamental lack of understanding. Everyone present seemed to agree that there is still a lack of understanding of many of the fundamental problems associated with the thin film semiconductor processing. Sustained research focus is needed in both the laboratory scale efforts to address fundamental issues and on the pilot line to address equipment and scale-up problems, in addition to validating processes.

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LIST OF FIGURES

Figure 1. Effect of selenization time on the efficiency of Cu(InGa)Se₂ devices made at EPV.