

CRITICAL ISSUES AND RESEARCH NEEDS FOR CdTe-BASED SOLAR CELLS

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ABSTRACT

We present a review of the basic features of polycrystalline thin-film CdTe solar cells and modules and then survey the outstanding fundamental issues and research challenges for application of this materials system to photovoltaic devices.

INTRODUCTION

Polycrystalline thin film cadmium telluride (CdTe) solar cells are one of the most promising candidates for large-scale application of photovoltaic energy conversion because they have shown laboratory efficiencies in excess of 15%^{1,2} and module performance of over 10%.³ In addition, CdTe solar cells with efficiencies over 11% have been made by a variety of deposition methods⁴, and several of these methods have been adapted to module manufacturing. Several good reviews exist of the deposition methods as well as module and device performance.^{5,6,7}

Progress towards improving device and module performance has been slow over the past five years and the translation of laboratory results to first-time manufacturing has been more difficult than expected due to the complexity of the processes involved for making large area, thin film CdTe modules. The slow progress is further compounded by the lack of the fundamental scientific and engineering knowledge base required to underpin the development of the technology. In this paper, critical issues are identified which have impeded the advancement of CdTe solar cell technology, and areas of basic research opportunities are identified.

All high-efficiency CdTe/CdS devices have been fabricated in a superstrate configuration as shown in Figure 1, where the CdS and the CdTe are deposited sequentially onto a glass/transparent-conducting-oxide (TCO) superstrate. Although there are variations in device fabrication process, particularly with respect to how the CdTe is deposited, it is possible to describe a "generic" fabrication procedure for high efficiency solar cells:

1. A glass superstrate is first coated with a TCO such as SnO₂ or indium tin oxide (ITO). The choice between ITO and SnO₂ is primarily determined by the deposition

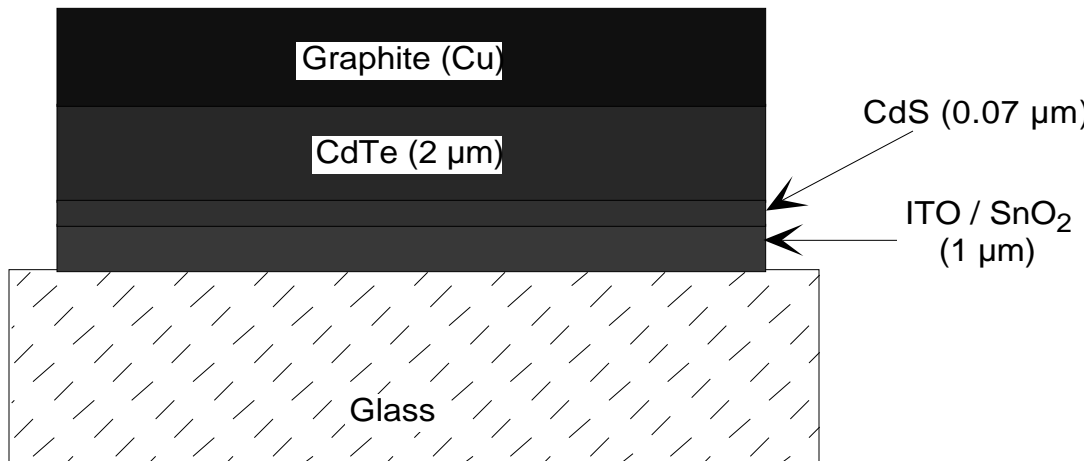


Figure 1. Basic CdS/CdTe cell structure.

temperature of CdS and/or CdTe films. For low temperature CdS and CdTe deposition processes, ITO is the material of choice, having higher optical transmission for a given sheet resistance. For CdS and/or CdTe deposition processes requiring high temperatures, SnO₂ is the best material since it is more stable, mainly due to the fact that the deposition process itself requires temperatures of 450 - 550 °C.

2. The CdS film is deposited by a wide variety of processes including close spaced sublimation (CSS), vapor transport deposition (VTD), chemical bath deposition (CBD), sputtering, screen printing, electrodeposition, atomic layer epitaxy (ALE), physical vapor deposition, and spray pyrolysis. For thin CdS, < 100 nm, the film is typically heat treated in a reducing atmosphere or in the presence of CdCl₂. The heat treatment increases grain size and may reduce the defect density of the films.^{8,9,10,11}
3. The CdTe film is deposited by a process such as close spaced sublimation, screen printing, spraying, electrodeposition, atomic layer epitaxy, physical vapor deposition, sputtering, chemical vapor deposition, molecular beam epitaxy, or laser ablation. Substrate temperatures are from 80 to about 630°C depending on the deposition process and the CdTe films are from 2 to 10 μm thick.
4. The CdTe/CdS structure is typically given a post-deposition heat treatment while exposed to CdCl₂ or another Cl containing compound such as Cl₂ or HCl.^{12,13} In some cases, such as in electrodeposition and screen printing, the chlorine may be contained in the original CdTe deposit.^{14,15} The heat treatment enables grain growth, reduces defect density in the films, and promotes the interdiffusion of the CdTe and CdS layers.^{16,17,18} The degree of diffusion varies among the various deposition procedures, but, for equilibrium conditions, it is limited by the miscibility gap between CdS and CdTe.^{17,18} In all cases the as-deposited thickness of the CdS layer is reduced and the CdS/CdTe interface becomes alloyed into a CdTe_xS_{1-x}/CdS_yTe_{1-y} interface, where x and y are less than or equal to the solubility limits at ~400 °C (x~0.03 and y~0.06).¹⁸
5. There is a wide diversity in structures and procedures for electrical contacts which generally includes at least two layers: the primary layer is a heavily doped or

degenerate layer that makes a low-loss electrical contact to the CdTe; and the secondary contact is metal or conductive ink that carries the current laterally. Most fabrication procedures include: an etch or surface preparation step, which may produce a Te-rich surface layer and remove oxides; creation of the primary layer, either by deposition of a p⁺-layer or ZnTe:Cu, HgTe or PbTe or by modification of the CdTe surface by supplying a p-type dopant; a subsequent heat treatment above 150 °C; and application of the secondary contact by sputtering, vacuum evaporation or screen printing.^{19,20,21,22,23,24,25}

From a device perspective, the thin film CdTe/CdS heterojunction devices show very low minority carrier recombination at the absorber grain boundaries and at the metallurgical interface which results in high quantum efficiencies. However, open-circuit voltages are relatively low due to recombination in the space charge region in the CdTe.

MATERIALS AND DEVICE PROPERTIES

In this section, we provide some additional details of the CdTe-related materials and devices with the objective of illustrating some of the complexity of these cells and describing some of the outstanding fundamental challenges which we believe impede progress in CdTe-based cell performance.

Device Model

The ideal one-dimensional device structure of Figure 1 may apply nicely to junctions in crystalline or epitaxial thin-film devices; however, it ignores the effects of grain boundaries and a variety of other complicating phenomena of the polycrystalline thin-film CdS/CdTe solar cell. A more realistic device structure is sketched in Fig. 2a where the

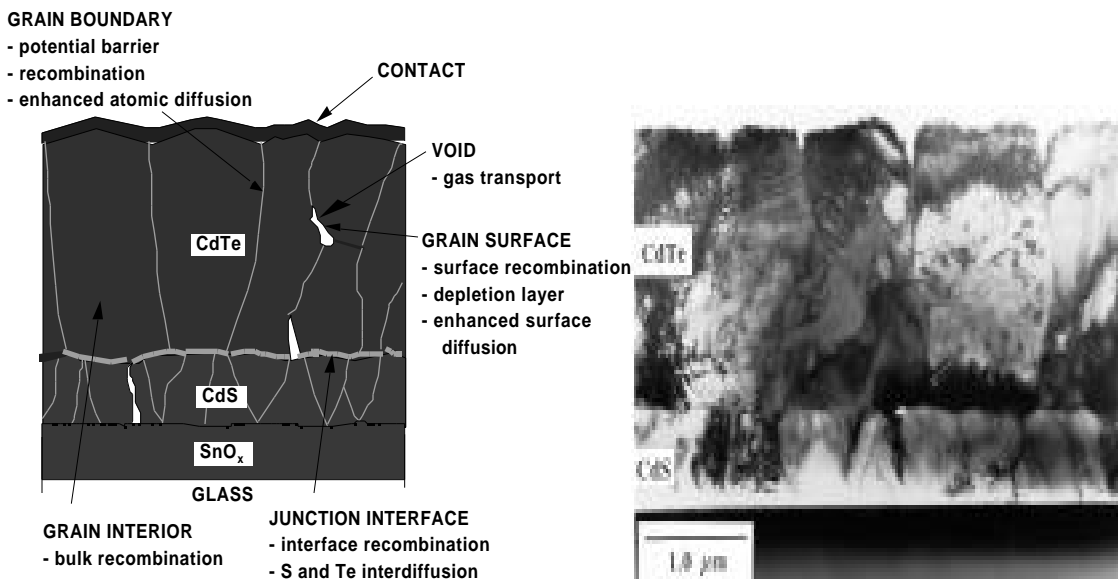


Figure 2. a) CdS/CdTe cell structure showing polycrystallinity and related issues; b) TEM cross sectional micrograph of a typical cell.

grain boundaries are displayed for CdS and CdTe layers. Note that there is a lattice mismatch of slightly greater than 10% at the heterojunction²⁶ so that epitaxial growth is necessarily limited. Successful device fabrication requires thorough understanding of, and

ability to control, the effects of grain boundaries, internal voids, possible pinholes through the thin CdS layer, interdiffusion across the CdS/CdTe interface, and the establishment of a low resistance contact without degrading the junction properties. The TEM cross-sectional micrograph of Fig. 2b illustrates the validity of this structural model.

Fig. 3 illustrates a structure with additional complexity, some aspects of which are certainly present. There is compelling evidence of interdiffusion at the CdS/CdTe interface forming a sulfur-rich layer of $\text{CdTe}_y\text{S}_{1-y}$ ($y \sim 0.03$) and a Te-rich layer of $\text{CdS}_x\text{Te}_{1-x}$ ($x \sim 0.06$).^{16,18} It has been proposed that this interdiffusion process results in S-rich spikes along the grain boundaries. This S-rich material is likely to be n-type and could lead to enhanced electron collection from the CdTe.

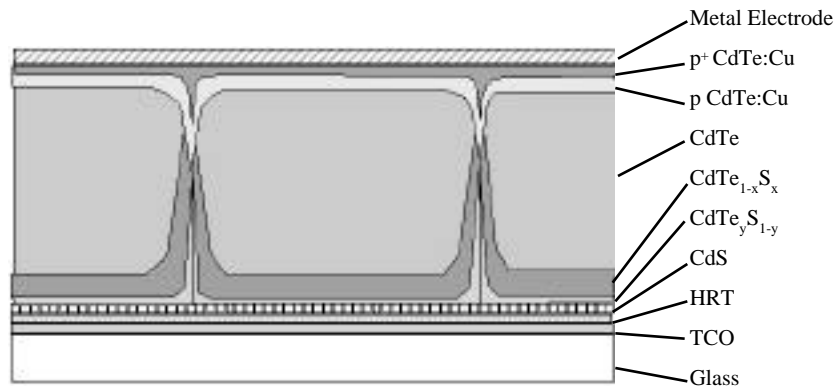


Figure 3. Further details of CdS/CdTe cell structure showing possible three dimensional effects. (From P. V. Meyers.)

In addition, the contacting process for the back of the cell cannot be assumed low resistance. It most commonly involves the creation of a heavily doped p-layer under the metal or graphite back contact. Such contacts sometimes produce a potential barrier high enough to produce non-negligible losses and can have stability problems. Nevertheless, more than one type of back contact has been shown to be sufficiently low resistance and to have excellent stability under cell²⁸ or module^{3,29} operating conditions. Finally, Fig. 3 shows the presence of a high resistivity tin oxide (HRT) layer between the TCO and CdS layers. A variety of HRT layers have been used^{30,31,32} and have been shown to improve device yield and may also enhance stability for some structures and under some stress conditions. Further discussion of the HRT layer is given later.

CdS/CdTe Interdiffusion

Some interdiffusion of S and Te across the metallurgical junction probably occurs during film growth, especially for the high temperature deposition processes. However, further interdiffusion occurs during the post-deposition treatment near 400°C in the presence of CdCl_2 or vapors containing Cl.^{12,13} In the blue from 400 to 500 nm, absorption in CdS attenuates the light reaching the CdTe layer, and thus reduces the quantum efficiency (QE) of the cell in this region. (No carrier collection appears to occur in the CdS, either because the minority carrier (hole) lifetime is too low or because other

factors present barriers to hole collection.) Note in Fig. 4 that, as the CdS thickness is reduced from 100 nm to 40 nm and to zero, the QE in the blue rises.

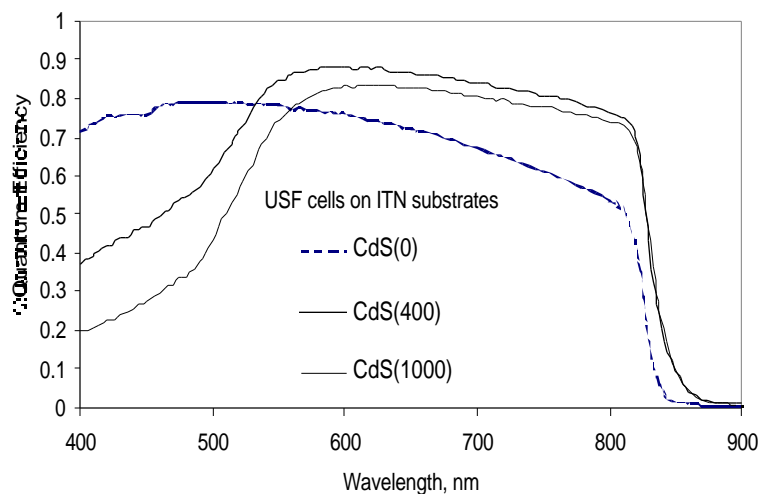


Figure 4. QE with and without CdS layers on substrates with an HRT layer as sketched in Fig. 3. Soda-lime glass/SnO₂ substrates from LOF; HRT deposited at ITN; cells fabricated at U. of South Florida.

The QE of Fig. 4 also shows evidence of the S-Te interdiffusion. The reduced QE between 520 and 580 nm provides *prima facie* evidence of interdiffusion of Te into the CdS. (The band gap shrinks at a rate of ~ 2.7 eV per unit y with increasing Te content in the CdTe_yS_{1-y}^{17,33}) Further evidence of interdiffusion arises from the red edge of the spectral response. When cells are fabricated with no CdS layer, the red edge of the QE lies at the band edge of pure CdTe (~ 820 nm). However, when cells are fabricated with some CdS, part of the CdS layer is consumed and the QE extends an additional 10 to 20 nm into the near infrared—in some cases up to 850 nm.³⁰ This is consistent with sulfur diffusion into CdTe, since the CdTe_{1-y}S_y alloy exhibits large band bowing.^{17,33} Other convincing evidence of the interdiffusion has been obtained with grazing angle x-ray diffraction.¹⁸

It should also be noted from the QE curves of Fig. 4 that the absence of an initial CdS layer reduces the overall quantum efficiency. There is some evidence that the use of an appropriate high resistivity TCO buffer layer (HRT) between the low resistivity TCO and the CdTe can permit the reduction of the CdS layer thickness to zero while maintaining high V_{OC}, provided that a low sulfur alloy, CdS_xTe_{1-x}, is used at least near the HRT interface.³⁰

Back Contacts with Copper

One of the most challenging aspects to the fabrication of high performance CdTe cells is the achievement of low resistance back contacts. The typical contact employs Cu in some way, presumably because the Cu diffuses into the CdTe producing a heavily doped p-layer. This has been accomplished by diffusion of Cu into CdTe and then deposition of a metal or carbon paint.^{19,21,23,24} Alternatively, the copper may be introduced by

mixing HgTe:Cu into the carbon paint which is then baked at temperatures up to 300 °C where some diffusion may occur.^{20,25}

As long as Cu is employed in the back contact structure, it will be critical to understand and control the role of Cu in CdTe. Some of the variety of effects are illustrated in the photoluminescence spectra shown in Fig. 5. These data were obtained on single crystal CdTe at 10 K but similar, although broader, features are observed from polycrystalline films.^{34,35}

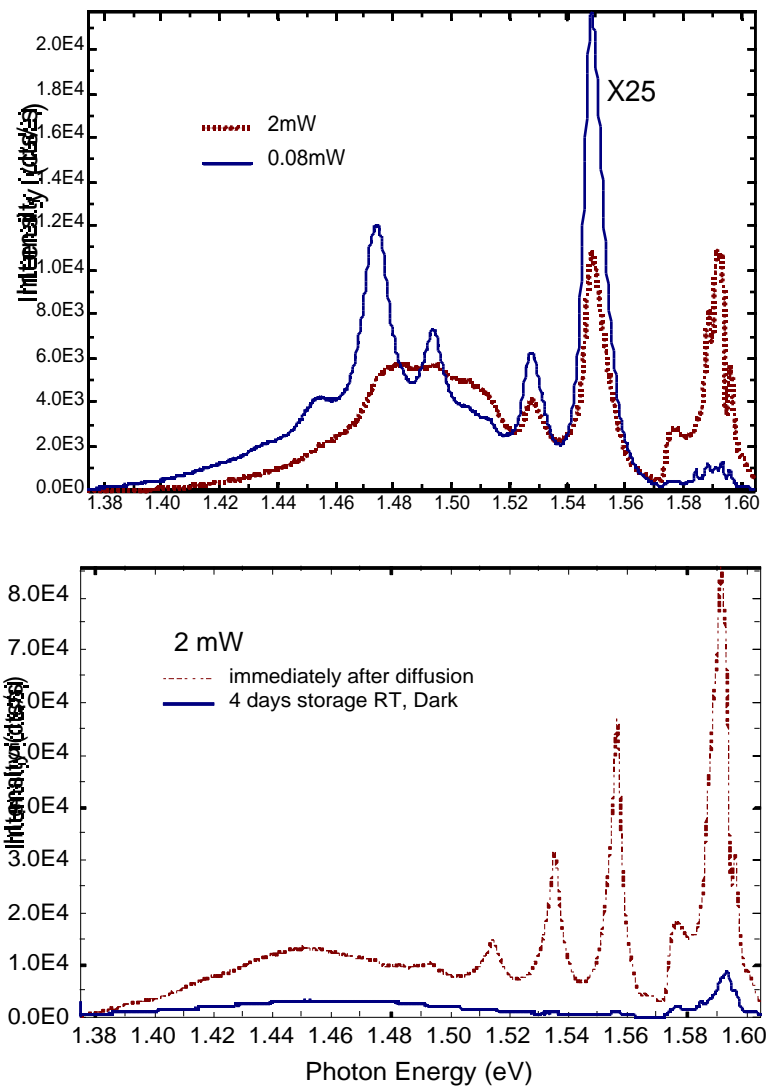


Figure 5. PL from crystalline CdTe at 10 K excited at 752 nm. a) Pure CdTe showing intensity dependence; b) under 300 K storage. 2 mW (0.08 mW) 0.5 mm spot.

10 K copper doped CdTe showing changes corresponds to about 10 (0.4) suns in the

Three types of features can be distinguished in the spectra:^{36,37} free and bound exciton-related peaks (1.575 – 1.60 eV), donor-acceptor (D-A) pair transitions from relatively shallow states (1.51 – 1.56 eV), and deeper lying D-A transitions (1.40 – 1.50

eV). The spectra depend strongly on the excitation power with exciton-related features dominating at high excitation powers due to the inherent bimolecular recombination. (See Fig. 5a.) At very low power, however, the D-A pair transitions dominate. Note that the transition near 1.55 eV shifts slightly to the blue with increasing excitation power. This is characteristic of D-A pairs due to the fact that the formation rate, the recombination rate, and the final state Coulomb energy (of the ionized donor and ionized acceptor) are dependent on the pair separation in the lattice.³⁸ Diffusion of Cu into CdTe quenches the shallow D-A pair (probably D- V_{Cd}) transition at 1.55 eV but produces a new peak near 1.45 eV (presumably D- Cu_{Cd}). Also Cu doping produces a dominant bound exciton peak near 1.59 eV (probably X- Cu_{Cd}). Additional Cu-related complexes form (possibly from combinations of Cu interstitials Cu_i , cadmium vacancies V_{Cd} , and/or substitutional copper Cu_{Cd}), which are quite unstable and disappear with time even at room temperature. These complexes have strong lattice coupling as seen from the optic phonon side bands in luminescence.

BASIC RESEARCH DIRECTIONS

There are several basic research issues that will quite likely have a direct impact on the continuing development of high-performance polycrystalline CdTe solar cells. At least some of these can be pursued with relatively straightforward measurement and analysis techniques. As with many polycrystalline materials systems, much of the challenge will be to develop a user-friendly shared data base from several systematic series of measurements.

Polycrystalline CdTe

The basic nature of polycrystalline CdTe has been elusive, and clearly more detailed knowledge is critical. What we know is that several deposition techniques yield similar quality solar cells, that the material used in cells has a low carrier density (10^{15} cm⁻³ range), that post-deposition annealing, generally with $CdCl_2$, can increase both crystallite size and hole density, and that the resulting structure resembles the one shown in Fig. 2. There is almost certainly a compensating process involving native defects, but at this point, there is no convincing description of the dominant process, or even strong evidence to decide whether it is associated with bulk CdTe or with granular surfaces. Theoretical evaluation of common possibilities involving vacancies, antisite doping, and simple complexes have recently been done with $CuInSe_2$ ³⁹ through calculation of the chemical potential as a function of Fermi level. Similar effort may provide useful insights for CdTe as well. Defect equilibrium models relating the densities of the various charged defects, dopant atoms, and free carriers have been done for p-CdTe:P in the past,⁴⁰ but the subject should be revisited with regard to CdTe with Cu, Cl, and O impurities.

Existing measurement techniques, such as photoluminescence, capacitance, DLTS, and lateral resistivity, can also be very powerful. They should incorporate systematic variation of temperature and illumination, and they should be applied to series of CdTe samples prepared with systematic variation of one or more process variables. Even better

would be improvement of techniques for making such measurements locally with high spatial resolution, so that one might have direct information to separate grain-boundary effects from those of the bulk. These measurements should be extended to other series of samples made with varying concentrations of extrinsic dopants and with alloys where Te is partially replaced with S and Cd with Zn. Virtually all solar cells show transient behavior of cell parameters to some degree. Although this has been explored for time scales of minutes to hours (*e.g.*, for CdS/CuInSe₂⁴¹), valuable information might be obtained by examining the transient behavior of the CdS/CdTe device on time scales from 10⁻⁶ sec to several seconds as a function of temperature and light intensity. In addition, it is important to map this territory in order to be sure that more routine testing is consistent. Finally, there should be major refinements of *in situ* process monitoring for both the vapor constituents and the growth surface. Greater assurance that the CdTe layer is uniform and reproducible will assist the measurement systematics, and may also lead directly to better performance cells.

CdS/CdTe Junction

Traditionally, n-CdS has been used to form a diode junction with p-CdTe, and the two materials, as shown in Fig. 1, have usually been viewed as separate layers. There is growing evidence, as shown in Fig. 3, that there is significant interdiffusion of S and Te in the completed diode. It is likely in fact that the degree and nature of this interdiffusion plays a major role in determining the actual junction location, diode quality, and cell performance. Again, a systematic series of samples, this time with the amount of interdiffusion used as the varied parameter, is recommended. The correlation of photovoltaic characterization with elemental profiles, morphology of the junction region, and post-deposition annealing should be helpful to our basic understanding of the diode junction.

The identification of specific dopant and recombination states in the CdS/CdTe-junction region is a difficult problem. It is also a critically important one, since these are the physical parameters that ultimately determine solar-cell performance. Theory may give some insight, but the most powerful experimental tool is likely to be photoluminescence (PL) with illumination through the CdS layer of completed cells. This configuration tends to be sensitive to the same region that controls the junction, and there have already been credible measurements of changes in peak height, peak position, local variations, and lifetime with post-deposition anneals.^{35,42,43} There needs to be a basic verification that PL, normally done at extremely high injection levels, indeed reflects the AM1.5 cell parameters accurately. Extension of the spectral range of PL to about 0.5 eV might yield additional information about midgap recombination centers (and check the common assumption that all recombination is non-radiative in this material). Finally, it would be very helpful to reduce or eliminate the use of relative units in PL spectroscopy measurements, making it possible to compare samples more productively. Three very practical questions are (1) whether industrial fabrication should be designed to explicitly incorporate a mixed CdS_xTe_{1-x} layer, (2) whether doing so might allow the elimination of a separate CdS layer, and (3) whether there may be alternatives to post-deposition annealing to achieve high performance. A more basic question is how is it that CdS

provides good junctions with CdTe. Is it poor band line-up between TCOs and CdTe? Is it passivation of recombination centers similar to the way S is used for surface passivation in the III-V system? Does interdiffusion act to getter defects near the junction? Or, does three-dimensional interdiffusion of CdS and CdTe create a favorable geometrical structure?

A very useful framework for comparison of different CdS/CdTe solar-cell results are computational simulations, based on carrier transport theory, using finite element mathematical techniques. Several user-friendly programs exist,⁴⁴ but they have been developed for one-dimensional analysis of single-crystal cells and need enhancements to account for polycrystalline features and for tunneling. In many cases the issue is whether the three dimensionality inherent in a polycrystalline structure can be reduced to a more manageable problem, such as separately lumping bulk and grain-boundary effects and then treating them in parallel. Creation of user-friendly two-dimensional simulators should be a priority.

Front Contact

Essentially all CdTe solar cells rely on a transparent conductive oxide, generally SnO₂, for the front contact. One goal is to minimize the product of the layer's electrical resistance and optical absorption, and basic work on the structure and properties of such oxides should be helpful. Perhaps more important, however, is the impact of the front contact, which is the first deposited layer in Fig. 1, on the rest of the cell. Variations in its morphology should be added to the list of parameters that are systematically correlated with cell performance.

Back Contact

The back contact for a CdTe cell, as suggested above, has been another of the major challenges, since the goal is a low resistance contact to a relatively wide band gap p-type material. Most of the successful solutions involve copper to form a thin p⁺⁺ or metallic-alloy layer on the surface of the CdTe, followed by a thicker conducting layer, such as the carbon shown in Fig. 1. The apparent problem is double-edged in that copper tends to diffuse away from the contact, leaving it more resistive, and towards the primary diode junction, decreasing its effectiveness. This thesis, however, is somewhat speculative, so better data on the actual profile of copper, and how it varies with CdTe deposition and contact formation techniques, as well as a theoretical model incorporating the effects of field-aided diffusion are needed. A different tack, which is already underway in earnest, is to find a copper-free contact strategy. The logical candidates are other p-dopants for CdTe, such as Hg, Ag, and Sb. Sb₂Te₃ shows good promise,²⁸ but it is too early to declare the problem solved.

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44. See, for example, AMPS-1D, a one-dimensional solar-cell simulation program written under the direction of Prof. S. Fonash at Pennsylvania St. Univ.