ANALYSIS OF STRESS-INDUCED DEGRADATION IN CdS/CdTe SOLAR CELLS

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ABSTRACT

Accelerated stressing of CdS/CdTe solar cells at elevated temperatures (60-100°C) under a range of applied bias in light and dark has identified three degradation modes: formation of a blocking contact, increased junction recombination, and increased dark resistivity. Devices with Cu-contacts degrade with a strong bias dependence. The blocking contact is formed under forward bias. Junction degradation requires both higher temperature and forward bias. Recontacting the device after stress removes the blocking contact with no change in junction losses. Devices without Cu in the contact have much poorer initial performance but degrade nearly independent of bias.

INTRODUCTION

CdTe/CdS modules in field testing scenarios are reported to be stable [1,2]. However, no clear correlation has been found between processing parameters and either these stable existence-proof cases or those that changed in field testing. Recent work to accelerate these processes at the laboratory scale (stress testing) have shown that typically the V_{oc} and FF degrades, particularly for devices held at moderate forward or reverse bias [3,4]. Also, there are reports of improvements that occur after relatively short periods [1, 4]. The back contact process is strongly implicated in the stress-induced degradation [4, 5], especially with respect to the presence of Cu and its compounds, which are sensitive to small, localized fields, in both electrochemical and electromigration processes [6]. A review of CdTe solar cell stability and the role of Cu has recently been published [7]. A difficulty in evaluating changes in device behavior is sample-to-sample variability in both CdS/CdTe films and post-deposition treatment and contacting processes. To minimize these variations, CdS/CdTe films from a single source were employed. In this paper, an analysis is presented of stress-degraded behavior, for devices made with 3 different back contact processes and stressed at different electrical bias points.

EXPERIMENTAL

Devices were fabricated using glass/SnO_2/CdS/CdTe layers supplied by First Solar LLC and back contact processes developed at the Institute of Energy Conversion (IEC). The “wet” process involves a bromine/dichrol/hydrazine etch, leaving a ~30 nm Te layer [8]. The “dry” process uses a Te vapor treatment to deposit a 10 nm Te layer [9]. Device contacting was finished with an evaporated Cu layer, (8-15 nm for the wet process and 2-6 nm for the dry process), followed by an application of Acheson 505SS carbon ink conductor. The initial efficiency of devices processed with Cu was 10 to 12%. Since Cu acts as both a p-type dopant and forms a Cu_2Te contact layer and can thus influence device operation in several ways, it was necessary to fabricate devices without Cu. In this case, the dry process was used to form the Te layer on which the carbon ink was applied. These devices exhibited lower V_{oc} and FF, blocking contact behavior, and initial efficiencies of 7 to 9%. It is important to note that, given the strong influence of contact processing on initial cell performance and stress-induced changes [4,5,9], the results on devices reported here are not representative of First Solar product using their contact.

IEC has constructed a system for stressing of CdS/CdTe solar cells by exposure to thermal, atmospheric, electrical, and illumination bias. Unique aspects of the equipment are: 1) controlled ambient conditions (dry bottled air, Ar, H_2/Ar or vacuum); 2) a wide range of active electrical bias; 3) T from 28-120°C; and 4) monitoring device performance *in-situ* during stress. No clear dependence on stress ambient was identified, so all devices reported here were stressed in dry air. Standard pumping and purging procedures were used to reduce gas phase contamination such as water vapor from the stress chamber before beginning the stress treatment. Electrical bias points used included reverse bias (RB) of –0.5V, short circuit (SC), maximum power (MP), open circuit (OC), and forward bias (FB) well beyond OC. Stress experiments were carried out for 10 days at 60° in dark or 100°C under ~1.2 suns.

EFFECT OF STRESS: PARTIALLY COMPLETED DEVICES

CdS/CdTe structures stressed at OC at 100°C without any contact layer (no Cu or C) yielded comparable performance (V_{oc}~0.80 V) to unstressed films once the contact was applied. CdS/CdTe structures were stressed at OC with a 6 nm Cu layer but no C contact at 100°C. The completed devices had V_{oc} ~0.65V. This indicates that the CdS/CdTe junction is intrinsically stable, and that the presence of Cu during stress is correlated with junction (V_{oc}) degradation.

SEPARATING CONTACT AND JUNCTION BEHAVIOR

A CdS/CdTe solar cell having an initial efficiency of 11.8% and V_{OC} of 0.82V was stressed at OC at 100°C for 6 weeks in air at 2 suns at Colorado State University. This reduced the efficiency to 7.2% and V_{OC} to 0.73V (Figure 1). J_0 increased by 30X, from 3E-8 to 8E-7 mA/cm^2, but there was no change in A-factor (~1.6), suggesting that the magnitude of recombination changes but not the mechanism (bulk recombination). This was confirmed with V_{OC}-T measurements. Figure 1 also shows that curvature develops after stress in both light and dark JV curves at forward bias, most likely due to a blocking contact. After stressing, the original carbon contact was removed, the CdTe surface was re-etched in weak bromine-methanol, and a new C contact was applied. The efficiency increased to 9.1% with no change in V_{OC}, J_0 and A. The blocking contact disappeared and the FF increased significantly. This clearly demonstrates that the curvature in forward bias is associated with the back contact. A contact barrier height of 0.3 eV has been determined after stressing [10].

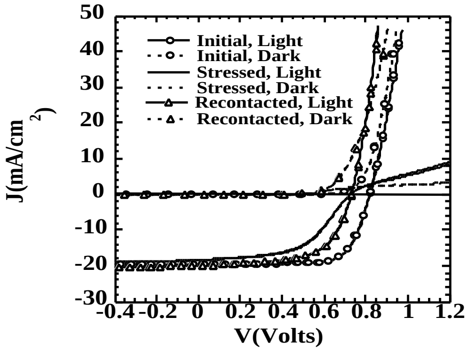

Figure 1. Light and dark JV curves for CdS/CdTe solar cell: initial; 6 week stress at 100°C at OC; and following re-contacting.

EFFECT OF ELECTRICAL BIAS AND Cu

Figure 2 shows the relative change in efficiency after stress as the ratio of efficiency after stress/before stress, for devices stressed at RB, SC, MP or OC for 10 days at 100°C in dry air. Devices with wet or dry contacts show similar changes with bias. Stress at SC always shows the least degradation in performance while stress at OC has the greatest degradation. Similar bias dependence has been found for cells with Cu that are stressed in H_2/Ar or Ar atmospheres, stressed at lower temperature (75°C) or have different Te layer processing. This non-monotonic behavior with bias suggests two different degradation processes for devices with Cu, whose combined impact has a minimum at SC bias stress. The error bars for the dry contact are based on a large number of samples and stress experiments. The variability in results is attributable to the interaction of process complexity with multiple degradation mechanisms. Devices without Cu degrade nearly independent of bias, and they have much less degradation at forward bias compared to devices with Cu. JV curves for devices biased at RB and SC behave similarly, while those at MP and OC have a different but common degradation mode. We simplify our discussion by considering two bias points, OC and SC. Figure 3 shows light and dark JV for devices stressed at OC and SC.

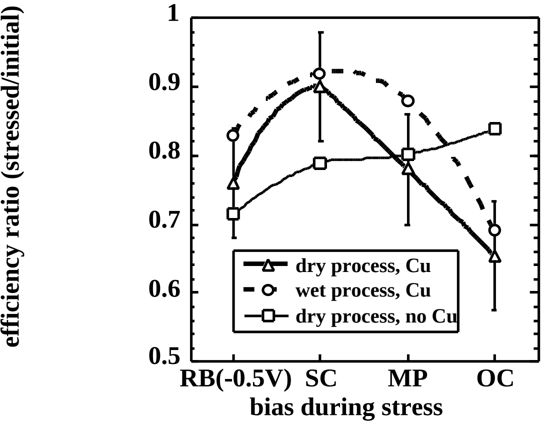

Figure 2. Relative change in efficiency for devices with different contacts after stressing at bias shown in light for 10 days at 100°C.

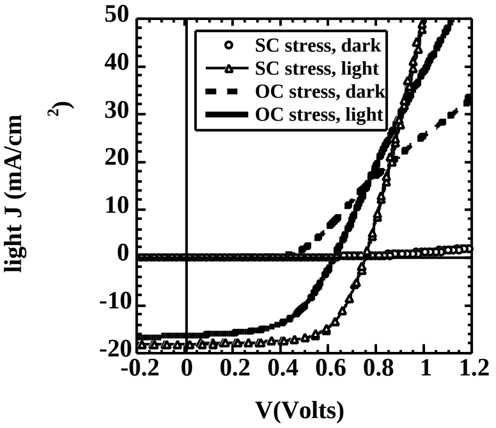

Figure 3. Light and dark JV curves after SC and OC stress for 10 days at 100°C. Dark curve for SC stress is nearly horizontal.

Devices stressed at SC have a smaller loss in V_{oc} (~50 mV) and FF (~5%) than those stressed at OC but develop a large cross-over between the light and dark curves, indicating a large photoconductivity effect. This has been attributed to formation of photoconductive Cu-doped CdS [7], although photoconductivity in CdTe cannot be excluded solely based on our measurements. Note that the formation of the blocking contact in Figure 3 was much weaker than in Figure 1, which is typical of cell-to-cell variability.

Since degradation was larger at OC than at SC, we extended the range of forward bias stress to 2.5 V. In this study, devices were in the dark to eliminate current flow at 0V. Figure 4 shows FF and V_{oc} for devices with and without Cu for stress in the dark for 10 days at bias from 0 to +2.5V at 60°C. There was negligible degradation for stress from 0 to 1V but significant change occurs for bias greater than 1V. V_{oc} and FF at 0V stress bias are essentially the same as the initial values. Devices with Cu show a strong bias dependence, with V_{oc} and FF decreasing similarly under forward bias. In contrast, devices without Cu degraded very little at any bias under these conditions. Note that the current density for devices with Cu was ~300 mA/cm^2 under +2.5V but ~100 mA/cm^2 for devices without Cu due to their current-limiting blocking contact.

DEVICE ANALYSIS : BIAS AND TEMPERATURE DEPENDENCE

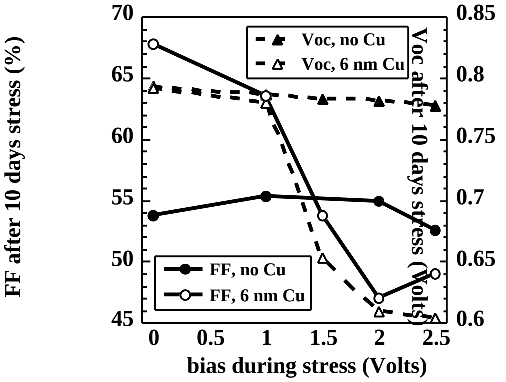

Figure 4. FF and V_{oc} for devices with 0 or 6 nm Cu for stress under FB in the dark at 60°C for 10 days.

The data in Figure 4 shows final performance after 10 days of stress at 60°C in the dark. In order to separate the effects of temperature, time and bias, the devices with Cu were initially stressed for one day at 28°C, then stressed for 1 day at 60°C, and then finally for the full 10 days. Then the device was recontacted as described above. The dark JV data has been analyzed by plotting dV/dJ vs 1/J as shown in Figure 5 for the device with +2V bias. The slope is AkT/q, the intercept is the series resistance R_S, and any curvature at large values of J at +2V bias, a significant blocking contact has developed which remained unchanged with further stress. Then, after 1 day at +2V at 60°C, the A factor and R_S increased, then remain unchanged for the next 9 days. After recontacting, Figure 5 shows that the blocking contact has completely disappeared but the increased A-factor and resistance remain unaffected (same as in Figure 1). This data indicates that degradation at forward bias occurs rapidly, even at 28°C, and the blocking contact is triggered by forward bias while the increase in junction recombination and resistance require elevated temperatures. These recontacting results from a device with a dry contact are in good agreement with the device of Figure 1 which had a wet contact and was

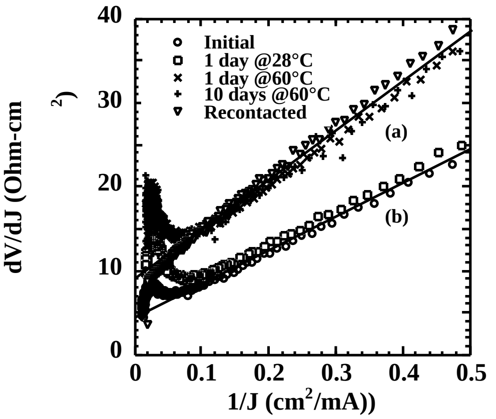

Figure 5. Analysis of dark JV curve as dV/dJ. The slope is AkT/q and the intercept is R_S, and curvature at large J indicates a blocking contact. (a) has A=1.6, R_S= 4 Ω-cm^2; (b) A=2.2, R_S= 9 Ω-cm^2.

stressed for longer times at a higher temperature at OC . The similarity in results with stress and recontacting strengthens the conclusions, discussed below. Devices on the same substrate as that shown in Figure 5 which were stressed at zero Volts showed no change in R_s, A or curvature with stress or recontacting.

MECHANISMS FOR DEGRADATION

We propose a model consistent with some but not all of the above results: devices with Cu under OC or forward bias degrade much more than under SC or 0V bias; degradation in V_{oc} or junction properties occurs rapidly (<24 hrs) even at 28°C; and a blocking contact forms to the CdTe. Using glancing incident x-ray diffraction at low incident beam angles to detect thin phases on CdTe surfaces before and after stressing, with contact removed, we have observed that the cuprous telluride present initially [10] is converted to cupric telluride after stressing. The Cu species liberated by this process are unaccounted for in our measurements. This relatively rapid change, together with the very small change at 0V, suggests that positive Cu ions could be generated and moved by field-driven diffusion along grain boundaries, or electromigration. This mechanism is discussed in detail in [7]. Positively charged Cu^{++} is available under bias by the weakly favored reaction:

$Cu_2Te \rightarrow CuTe + Cu^{++} + 2e^-$, with $\Delta G_{100C} = -0.7$ kcal/mol.

Note that while Cu_2Te is a highly conductive p-type material and makes a good ohmic contact to CdTe, CuTe is a poor conductor and could be responsible for the blocking contact.

However, there are several observations which are inconsistent with the electromigration of Cu along grain boundaries. It fails to explain why Cu-free devices degrade, why degradation isn't monotonic with bias (SC is most stable bias), or why large photoconductivity develops for stress at SC or RB. Also, the back contact barrier opposes that of the main junction, leading to Cu ions drifting in the opposite direction at the back compared to the CdS junction at a given bias. Thus, while electromigration of Cu along grain boundaries is a plausible mechanism, it is certainly not the only one responsible.

PHENOMENOLOGICAL MODEL AND CONCLUSIONS

We have shown that there are at least 3 mechanisms operative in CdS/CdTe devices under thermal and bias stress. One, which occurs at forward bias, is Cu-related, field-driven, occurs in ~hours, greatly increases the recombination, and is partially reversible with field [7, 13]. A second mechanism leads to formation of a blocking contact which also occurs rapidly and is likely related to loss of Cu, but is not reversible with field. It is eliminated by replacing the contact without additional Cu. The third mechanism, which occurs under reverse bias, is much slower, may not be Cu related, and changes the photoconductivity of either the CdS or CdTe. We propose that Cu^{++} is liberated from the Cu_2Te layer and moves along grain boundaries under forward bias. The concentration-gradient driven diffusion lengths (using D values from [12]) for Cu in bulk CdTe and along grain boundaries have been calculated for 1 hour at 100°C. Cu would move 0.3 µm in the bulk and 30 µm along grain boundaries. Clearly, grain boundaries are important channels for Cu motion.

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