

# TEXTURING FOR HETEROJUNCTION SILICON SOLAR CELLS

Matthew B. Edwards, Stuart B. Bowden and Ujjwal K. Das  
Centre of Excellence for Advanced Silicon Photovoltaics and Photonics  
University of New South Wales, Sydney NSW 2052, Australia, email: me@pretzelcorp.com  
Institute of Energy Conversion  
University of Delaware, Newark DE 19716, USA

**ABSTRACT:** Heterojunction solar cells have potential for very high device voltages and currents, yet this relies on correct preparation of wafer surfaces prior to a-Si deposition. This paper investigates the preparation of wafer surfaces by NaOH texturing prior to amorphous silicon intrinsic layer deposition. It is found that with a CP etch or low temperature anneal after texturing, and with correct deposition parameters, effective wafer lifetimes in excess of 1 ms can be achieved, indicating excellent surface passivation. Low reflectance achieved following wafer texturing along with high wafer lifetime led to efficiencies in finished devices as high as 17.6%.

**Keywords:** Heterojunctions, texturisation, passivation

## 1 INTRODUCTION

Silicon heterojunction (SHJ) solar cells based around amorphous silicon (a-Si) on crystalline silicon (c-Si) have demonstrated high efficiencies without requiring high temperature processing [1]. Low temperature processing maintains high bulk lifetime so that finished devices are limited by surface recombination. Good passivation of wafer surfaces becomes critical in allowing high device voltages to be realised. In the past, excellent surface passivation and cell performance has been achieved on wafers with advanced surface treatments such as anisotropic texturing, achieving high currents without compromising device voltage and resulting in published efficiencies exceeding 20% [2].

The performance of a silicon heterojunction solar cell is largely governed by the defects at the interface between the a-Si and c-Si. Performance is improved by reducing defects at the interface by inserting a thin, a-Si intrinsic layer (i-layer) between the doped p-type a-Si emitter layer and the n-type c-Si substrate [3,4]. However, surface contamination on the silicon substrate before deposition of the a-Si layer will increase the interface defects and reduce the cell performance.

Texturing is important for improving device current output by reducing surface reflection. In this study, we investigate the effects of anisotropic texturing on the lifetime and cell performance of heterojunction device structures with a-Si i-layer. Where negative effects on wafer lifetime are encountered, methods to alleviate lifetime degradation after surface treatment are investigated. These methods include isotropic etching to remove metallic contamination prior to a-Si deposition and annealing of deposited i-layer films. Anisotropic texturing is shown to be compatible with high wafer lifetime and open circuit voltage in a-Si/c-Si heterojunction devices.

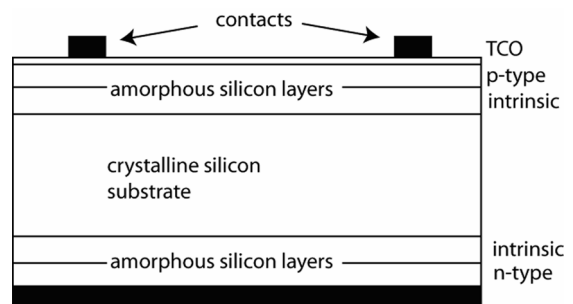
## 2 EXPERIMENTAL PROCEDURE

N-type, Cz and FZ wafers with <100> orientations were subjected to random pyramid texturing, using a 2% NaOH solution with 2-propanol added as a wetting agent. Following treatment in NaOH, the wafers underwent an RCA2 clean, a short chemical polish (CP) etch, or both. The RCA2 solution consisted of 6:1:1 H<sub>2</sub>O:HCl:H<sub>2</sub>O<sub>2</sub>, heated to ~ 80°C for 5 minutes. The CP etch consisted of

300 mL HNO<sub>3</sub>, 100 mL CH<sub>3</sub>COOH and 40 mL HF and varied in duration from 0 to 60 s. Reflectance measurements of the wafer surface were made following the CP etch.

Following surface treatment, wafers were cleaned in H<sub>2</sub>SO<sub>4</sub>/H<sub>2</sub>O<sub>2</sub> followed by an HF dip. The samples were immediately transferred to the deposition system and an intrinsic a-Si layer deposited on both sides of the wafer to a thickness of ~10 nm. The deposition occurred through a plasma enhanced chemical vapour deposition (PECVD) process and with hydrogen to silane dilution ratio R = 2. Following i-layer deposition, wafers were annealed at ~ 300°C in air for times varying from 0 to 70 mins.

The wafers were then transferred back into the PECVD system for deposition of a p-type doped a-Si layer on the front and an n-type doped a-Si layer on the rear. Finally, the contacts were added, consisting of a transparent conductive oxide and Ni/Al grids on the front, and a full coverage of Al on the rear. The resulting device is pictured in figure 1.

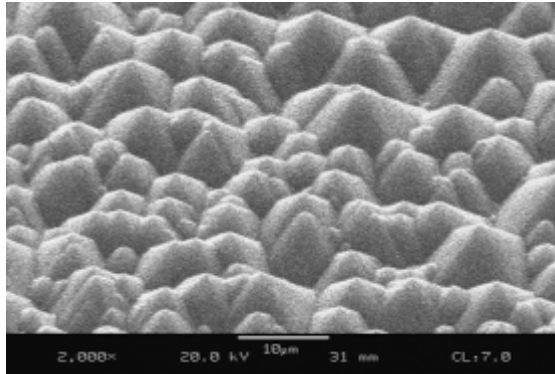


**Figure 1:** Schematic of final cell structure

Effective minority carrier lifetime was measured using an inductively-coupled photoconductance bridge [5]. The lifetime measurements were used to assess the quality of surface passivation following each of these processing steps, and to assess the suitability of each of the particular surface preparations prior to a-Si deposition. All lifetimes quoted are at a minority carrier injection level of 10<sup>15</sup> cm<sup>-3</sup>.

### 3 RESULTS AND DISCUSSION

Random pyramid texturing was achieved on high lifetime n-type Cz wafers using weak NaOH solution with a strong sodium silicate concentration [6]. Small amounts of 2-propanol were added as a wetting agent, since silicate rich NaOH tended not to wet the surface of the wafers. Figure 2 shows an SEM image typical of the textured n-type Cz wafers in this study. The reflectance was 11.6% at 700 nm incident wavelength.

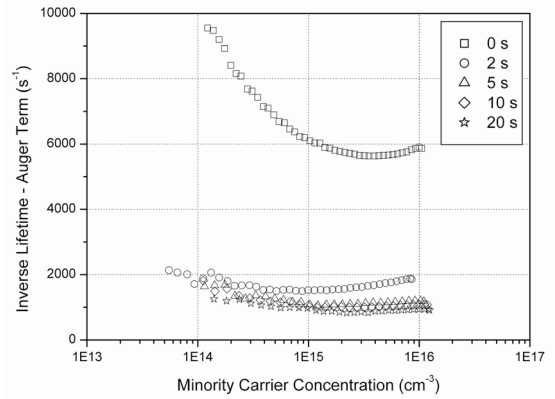


**Figure 2:** SEM image of random pyramid textured wafer typical of those used in this study, magnified 2000X.

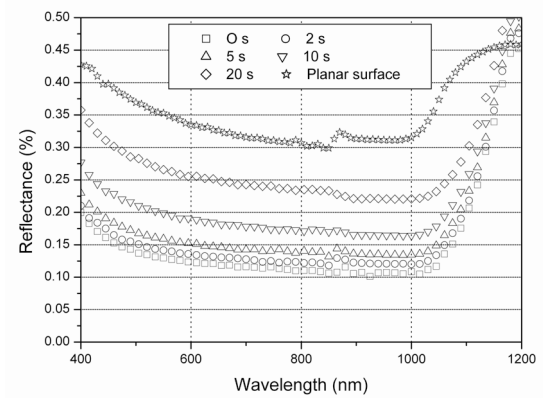
The lifetime of the textured wafer sample after RCA2 cleaning and deposition with a-Si was only 192  $\mu\text{s}$ . Much higher lifetimes were achieved on textured wafers CP etched prior to a-Si deposition. Figure 3 shows the increase in lifetime with increasing CP etch time. High lifetimes (up to 1074  $\mu\text{s}$ ) are achievable but the reflectance also rises to high levels. There is a trade off between high  $V_{oc}$  (due to improved lifetime at long etch times) and high  $J_{sc}$  (due to better texture at short etch times). A short CP etch of 5 s resulted in an acceptably high lifetime of 899  $\mu\text{s}$  but with only a slight increase in the reflectance to 14.3% at 700 nm as shown in figure 4. The reflectance was considerably lowered through the later application of anti-reflection coatings.

The increase in lifetime from CP etching prior to a-Si deposition is due either to a reduction in stress in the deposited i-layer by the slight rounding of the pyramid peaks or a reduction in Na at the c-Si/a-Si interface. XPS analysis of NaOH-treated Si wafers indicates that significant Na can remain close to the surface of the wafer even after RCA2 cleaning, and that this Na can be removed by a short CP etch [7].

Figure 5 shows lifetimes of textured, n-type Cz wafers with deposited i-layer following a series of anneals at  $\sim 300^\circ\text{C}$  in air. A clear benefit in annealing the deposited films is evident, particularly for samples not undergoing CP etching prior to i-layer deposition. Lifetime rose from 162  $\mu\text{s}$  to 702  $\mu\text{s}$  after 70 minutes of annealing in this case, making the wafer lifetime comparable to samples that had been CP treated. For samples CP etched for short periods of time, best results were generally seen after only 20 minutes of annealing, with wafer lifetimes rising between 30% and 100%.

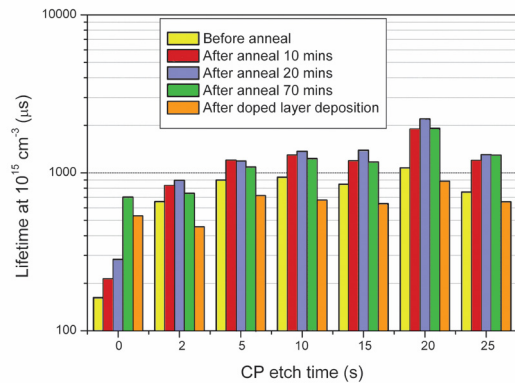


**Figure 3:** Inverse-lifetime curves for textured n-type, Cz wafers with a-Si i-layer, for varying post-texture CP etch durations.



**Figure 4:** - Reflectance curves for textured n-type, Cz wafers, for varying post-texture CP etch durations.

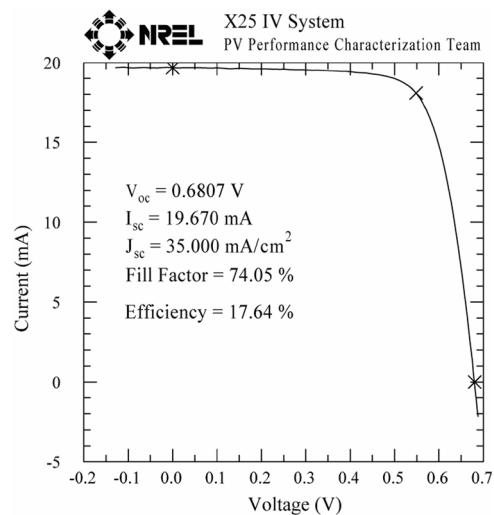
For cells that were annealed for 70 minutes following i-layer deposition, and did not undergo CP etching following texturing, actual open circuit voltages were as good or better than cells that did undergo CP treatment, without any loss of short circuit current. However, short CP etches of 5 to 10 s result in lifetimes approaching 1 ms after a-Si deposition, with only minimal short circuit current loss. Either method may be used to obtain good surface passivation and finished cell performance, increasing the flexibility of the process.



**Figure 5:** Lifetimes at carrier concentration  $10^{15} \text{ cm}^{-3}$  for textured n-type, Cz wafers with a-Si i-layer, for varying post-deposition anneal duration. Lifetime after doped emitter layer deposition is also shown.

Lifetimes of textured Cz wafers were significantly higher than those of planar  $\langle 100 \rangle$  Cz wafers, reaching  $1074 \mu\text{s}$  at  $10^{15} \text{ cm}^{-3}$  without annealing, whereas the planar wafers reached only  $229 \mu\text{s}$  at  $10^{15} \text{ cm}^{-3}$ . This difference is due to the relative difficulty in achieving amorphous silicon growth on  $\langle 100 \rangle$  surfaces compared to  $\langle 111 \rangle$  surfaces [8], observed on planar wafers. The deposited layer needs to be wide bandgap a-Si for passivation. If epitaxial growth occurs, the deposited layer has the same bandgap as the silicon wafer. Since the epitaxial layer is highly defective with low doping there is no barrier to minority carriers and high recombination results. Since texturing exposes  $\langle 111 \rangle$  planes, it might be concluded that anisotropic texturing of  $\langle 100 \rangle$  wafer surfaces, or use of  $\langle 111 \rangle$  oriented wafers, is highly beneficial in heterojunction solar cell processing [8].

Using the texturing technology and anneal process developed in this study we have demonstrated cells with an independently confirmed efficiency of efficiency of 17.6% as shown in figure 6. The device displays a high  $V_{oc}$  for a textured cell at 681 mV. The same device was independently measured to have a  $V_{oc}$  of 688 mV when the measurement mask was removed, indicating that the cell has significant edge recombination. Later devices measured efficiencies over 18% but are yet to be confirmed. Efficiencies of 21% [2] achieved on textured, heterojunction silicon solar cells suggest that very high voltages and currents are achievable in practical devices. The above results show that good wafer lifetimes along with optical performance on relatively low quality silicon are easily achievable given the correct processing conditions.



**Figure 6:** JV curve of confirmed efficiency solar cell.

#### 4 CONCLUSION

In heterojunction solar cells, effective preparation of textured wafer surfaces prior to a-Si deposition and correct deposition parameters allows good cell performance to be achieved. A short CP etch of 5 to 10 s following NaOH texturing was found to allow for excellent surface passivation, with only minimal increase in reflectance due to pyramid rounding. A low temperature ( $\sim 300^\circ\text{C}$ ) anneal in air for 70 minutes, following texturing, was found to allow excellent passivation of wafers that had not undergone CP etching. The anneal also presents no risk of damage to the textured surface, allowing low reflectances achieved during texturing to be maintained in finished solar cells. It was also found that  $\langle 111 \rangle$  surfaces exposed during texturing were passivated more effectively than  $\langle 100 \rangle$  surfaces, making texturing highly beneficial for both device voltage and current. Correct preparation of wafer surfaces can lead to excellent heterojunction solar cell efficiencies, with 17.6% achieved in this study.

#### 5 REFERENCES

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