

# A-SI/C-SI HETEROJUNCTION FOR INTERDIGITATED BACK CONTACT SOLAR CELL

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**ABSTRACT:** An interdigitated back contact silicon heterojunction solar cell is discussed, which combines the high voltage potential of heterojunction solar cells while avoiding the absorption losses in these structures which allowing high short circuit currents. This structure has interdigitated p/n amorphous silicon (a-Si:H) films deposited by low temperature plasma enhanced chemical vapor deposition on the backside of crystalline silicon (c-Si) wafers, with the light irradiating the front surface. The device is attractive for manufacturing due to the all back contact design, the large tolerances in dimensions, low temperature of depositions, and the lack of shunting. Initial solar cells have open circuit voltages of 691 mV but low fill factors. Two-dimensional modelling is used to explain the present low fill factors and demonstrate that the structure allows efficiencies in excess of 24%.

**Keywords:** c-Si, heterojunction, back contact

## 1. INTRODUCTION

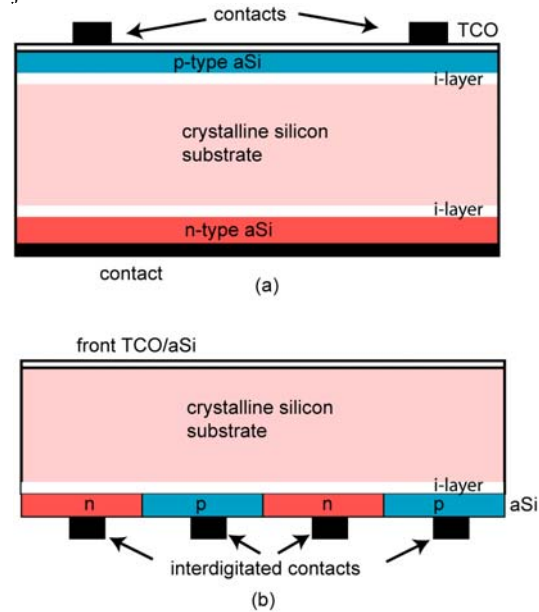
Rear junction, interdigitated back contact (IBC) solar cells (e.g. Figure 1b) have several advantages over the more common front junction solar cell with contacts on either side (e.g. Figure 1a). Moving all the contacts to the back of the cell eliminates contact shading, leading to a high short-circuit current ( $J_{SC}$ ). With all the contacts on the back of the cell, series resistance losses are reduced as the trade-off between series resistance and reflectance is avoided and contacts can be made far larger. Having all the contacts on the one side simplifies cell stringing during module fabrication and improves the packing factor. The reduced stress on the wafers during interconnection improves yields, especially for large thin wafers. The more uniform appearance of the PV module is desirable for architectural applications.

While the advantages of rear junctions are well known, their implementation is hindered by several design constraints, which are circumvented by amorphous silicon on crystalline silicon heterojunctions. First, since rear junction cells require diffusion lengths greater than twice the device thickness, thin wafers are attractive. Using low temperature depositions rather than high temperature diffusions decreases the thermal stress and reduces the bowing in thin wafers. Deposition temperatures are also low enough to prevent impurity indiffusion and maintain high initial lifetime of n-type substrates. Second, rear junction designs require low front surface recombination velocities, which can be provided by deposited passivation layers. Thirdly, the central challenge in rear junction solar cells, patterning the rear, is easier in silicon heterojunctions since it is much easier to mask and etch depositions than diffusions, and further isolation between p/n a-Si layers is not always necessary.

All back contact cells are particularly suited to heterojunctions as they eliminate the costly front transparent conductive oxide (typically indium-tin-oxide) along with its absorption losses. Interestingly, with the heterojunction material on the rear, it no longer needs to be transparent and thus there is a wider flexibility in choosing heterojunction partner materials as not all wide band gap semiconductors are completely transparent.

The interdigitated back contact silicon heterojunction (IBC-SHJ) devices described in this paper potentially

combine the advantages of the two leading high efficiency technologies, namely, the high  $V_{OC}$  of heterojunction cells and the high  $J_{SC}$  and FF of rear junction cells.



**Figure 1:** (a) Standard front junction design. (b) Rear junction design with interdigitated back contacts (IBC-SHJ). Devices are fabricated with and without the intrinsic buffer layers between the doped a-Si and c-Si.

## 2. DEVICE PERFORMANCE

### 2.1. Device structure

The IBC-SHJ device consists of a 1-3 ohm.cm, 300 $\mu$ m thick, n-type float zone c-Si substrate with rear interdigitated strips of n and p amorphous silicon, with widths of 0.5 mm and 1.2 mm respectively. The amorphous silicon is covered with aluminium metal as robust contacts. The front surface of the substrate is passivated with intrinsic amorphous silicon layer followed by anti-reflection coating. All amorphous silicon depositions are performed in DC plasma enhanced chemical vapour deposition (PECVD) system at 170°C. We have also used RF plasmas (13.56 MHz) but find little practical difference [1]. Presently the interdigitation

is achieved through the use of photolithography, but the large millimetre-sized dimensions allow for other options to be investigated.

## 2.2. Device without rear intrinsic layer

Initial heterojunction back contact cells were fabricated using doped layers only on the back. Without an intermediate intrinsic a-Si buffer layer, the  $V_{OC}$  is limited to around 600 mV [2-3], but the cell optimization is more straightforward since the i-layer often reduces the fill factor (see next section). Using the doped only contacts, the device had an efficiency of 11.8%,  $V_{OC}$  of 602 mV,  $J_{SC}$  of 26.7 mA/cm<sup>2</sup> and FF of 73% [4]. Notably the device has a high shunt resistance, showing that it is straightforward to separate the heavily doped p and n contact regions with a silicon heterojunction, unlike the diffused-junction devices [5] where shunting is more likely to happen.

Texturing the substrate and improving the front AR coating (presently absorbing ITO) will increase the current. We have applied texturing to our front junction cells and increased the current by 10% and the  $V_{OC}$  only falls by 10 mV.

## 2.3. High $V_{OC}$ with intrinsic layer

The device reported in the previous section was fabricated without the use of an intrinsic amorphous silicon buffer layer. The absence of the buffer layer simplifies fabrication, and ensures a high fill factor, but increases the recombination at the amorphous silicon/crystalline silicon interface. Much higher  $V_{OC}$ 's are attainable if an intrinsic buffer layer is inserted between the doped a-Si and the c-Si substrate. For example, on standard front junction SHJ devices at IEC (Figure 1a), we have obtained a  $V_{OC}$  of 703 mV with an intrinsic buffer layer, but only 622 mV without the buffer layer.

For IBC device, inserting an i-layer at the rear increased the  $V_{OC}$  from 602 mV to 691 mV (Table I), and compares favorably with the 681 mV obtained by Sunpower on their record rear junction device. However, a disadvantage of inserting the intrinsic buffer layer is that it can reduce conduction of carriers and lead to low fill factors. Front junction cells fabricated at IEC initially had the same problem of very low fill factors, however, optimization of the i-layers enabled the fill factors to exceed 70 % with only a slight drop in  $V_{OC}$ , from 703 mV to 693 mV, and efficiency of 18% has been obtained.

**Table I:** Effect of intermediate buffer layers of  $V_{OC}$ 's on front and rear heterojunction devices.

Cell	$V_{OC}$ (mV)
Front Junction (no i-layer)	622
Front Junction (i-layer)	703*
IBC (no i-layer)	602
IBC (i-layer)	691

\*Textured Cz substrate. Other substrates are planar FZ.

## 3. TWO DIMENSIONAL CELL MODELING

### 3.1 Modelling description

The interdigitated back-contact heterojunction device combines two technologies with challenging modelling requirements. Firstly, an all back contact device is an inherently two-dimensional structure that is difficult to

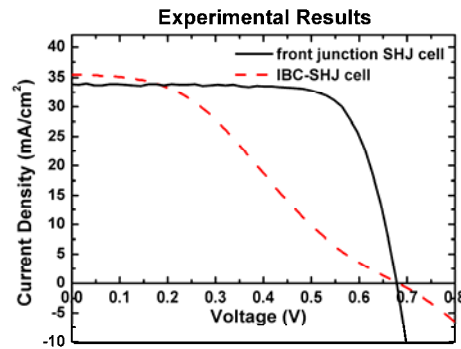
model analytically or using a standard one-dimensional program such as PC1D. Secondly, heterojunction devices incorporating amorphous silicon have also proven difficult to model, often requiring the development of new modelling programs.

The Sentaurus device modelling package is extensively used for modelling opto-electronic devices and is suited for modelling solar cells through the inclusion of DESSIS. The latest version includes complex defect models allowing the simulation of devices including amorphous silicon. The critical parameters included in our study are energy distribution of the exponential band tails, and the Gaussian distribution of the mid-gap trap states. These are essential for the accurate modelling of any amorphous silicon device. In simulation, they are chosen based on reference [6] and were tuned to fit the experimental properties (e.g. band gap, dark and light conductivity) of our deposited a-Si layers. A further benefit of the Sentaurus pack is that it includes realistic optical effects such as absorption in the amorphous layer.

### 3.2 Fill factor losses in IBC-SHJ

To determine the origin of the fill factors in the back contact cells with i-layers, two cells following the schematics of Figure 1 were made with identical amorphous silicon deposition conditions. In both cells, there is a 10 nm i-layer inserted between the doped a-Si layers and the c-Si substrate.

As demonstrated in Section 2.3, the insertion of an intrinsic layer at the heterojunction interface increases the  $V_{OC}$  for both the front and rear junction devices. However, while the fill factor of front junction cells are relatively unchanged, the fill factor on IBC-SHJ devices dropped dramatically from 73% to 37%. The loss of fill factor is shown in the JV curves of Figure 2. The JV curve is flat into reverse bias indicating that the loss in fill factor is not due to shunting between the n and p strips. Successive runs using similar conditions showed that low fill factors are more of a problem with IBC-SHJ cells than with the front junction devices.

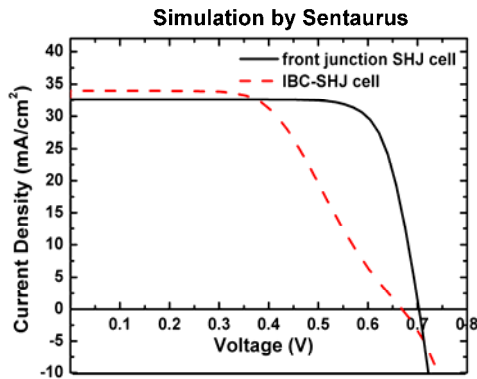


**Figure 2:** Measured JV curves for front and rear junction solar cells. The i-layer has the same thickness of 10 nm in both devices.

The front-junction and IBC devices of Figure 2 were both modelled with Sentaurus and are presented in Figure 3. The simulation conditions, hetero-interface model and the material properties of doped a-Si, intrinsic a-Si, c-Si wafer, for both devices are identical except the structure

itself. The results match the experimental data with a fill factor drop evident in the IBC cell but not in the front junction cells.

There are a number of possible causes for the large difference in FF between the two devices. The current density is higher at the interface in the IBC cells as the interdigitation of the contacts means that approximately half the area is available to each contact. A more likely cause is the effect of the illumination on the i-layer due to photoconductivity of the intrinsic a-Si or changing the band alignment at each interface. Most of the light is absorbed at the front surface, so that the carrier concentration at the junction in a front junction device is far larger than the carrier concentration at the junction for the IBC cell. Finally, the IBC device has the n and p aSi regions in close proximity and the FF loss could be due to conduction through the p-i-n structure and associated crystalline silicon region.



**Figure 3:** Modelling of front and rear junction cell with Sentaurus. The loss in fill factor on the IBC-SHJ cell matches the experimental results in Figure 2.

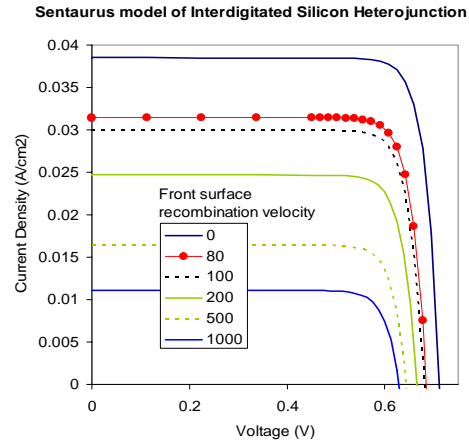
The S-shaped curve present in the IBC-SHJ cell is similar to those seen for front junction cells that were obtained when the i-layer is too thick or the surface at the interface is contaminated. We achieved an improvement in the front junction cells by changing the processing steps and deposition conditions of the a-Si layers. Similar optimizations of IBC-SHJ solar cells are ongoing.

### 3.3 Front surface passivation

The performance of IBC-SHJ solar cell depends on the front surface passivation [4]. Simulation of an IBC-SHJ solar cell without back surface intrinsic a-Si layer but with different front surface recombination velocity  $S$  was performed, and the resulting J-V curves are shown in Figure 4. As seen, both  $J_{SC}$  and  $V_{OC}$  increase as  $S$  decreases, resulting in higher cell efficiency. Since most carriers are generated near the front surface, while the p-n junction is far at the back surface, high front  $S$  would cause carrier recombination before they reach the back junction.

Further, the Sentaurus modelled JV curve can also be used to extract the front surface recombination velocity if good back surface passivation is assumed instead of inserting the i-layer. In Figure 4, the front surface recombination velocity  $S$  of 80 cm/s (line with dots) provides a good match to the experimental device with i-layer. This  $S$  value is consistent to the surface

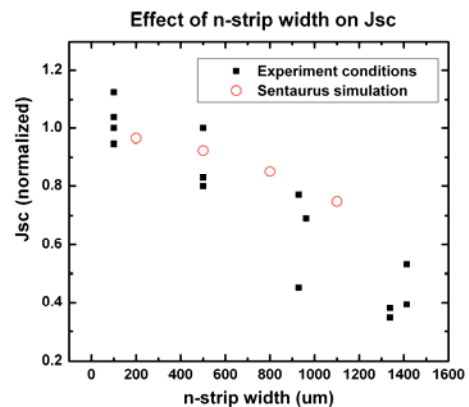
recombination velocity of 82 cm/s extracted from IQE curve by using PC1D [4].



**Figure 4:** Sentaurus modelling of an IBC-SHJ solar cell. The line with dots shows the fit to the device with i-layer device indicating that the front surface recombination velocity is 80 cm/s.

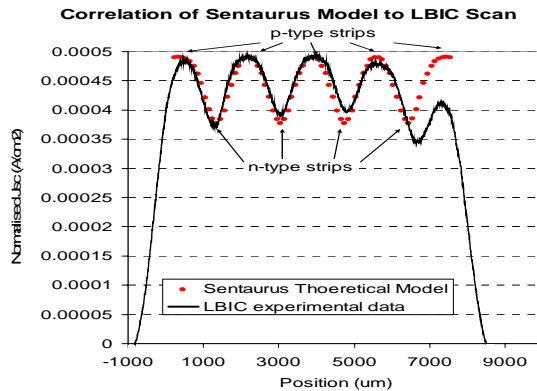
## 4 EFFECT OF STRIP DIMENSIONS ON IBC-SHJ PERFORMANCE

Sentaurus modelling was also used to assist in the optimization of the dimensions of the back contact strips. There is a trade off in the relative sizes of the strips. The recombination at the p-type collecting junction is higher than at the n-type passivation but carriers generated above the n-type strips have to travel further to reach the collection junction. There is thus a trade off in the relative sizes of the p and n strips. Due to resistive parasitics caused by the i-layers, the strip optimization was performed on devices without the intermediate i-layer on the back of the cells.  $J_{SC}$  is normalised to account for differences in front surface reflection and absorption in the ITO which is present in the actual cells but not in the model.



**Figure 5:** Correlation of simulated and measured result on the effect of the width of n-strips on  $J_{SC}$ . The total device dimension is fixed so wider n-strips result in narrower p-strips.

The optimization of the strip width is shown in Figure 5. The simulation was performed by keeping the total device dimension fixed, hence wider n-strips result in narrower p-strips. It can be seen that for the passivation conditions used in simulation (which matches experiments), as n-strip width increases,  $J_{SC}$  decreases, resulting in lower cell efficiency. The optimal width of the aSi n strip is as narrow as possible with the limit provided by the limit of alignment technology.



**Figure 6:** The Sentaurus theoretical model matches the experimental data from a LBIC scan, validating the 2D model.

To further investigate the device performance, a cell was measured using light beam induced current (LBIC) and compared to the theoretical calculations from the Sentaurus two dimensional computer simulation as shown in Figure 6. The base wafer is n-type so carriers generated at the p-type strips with the collection junction are much more likely to be collected than carriers above the n-type strips, which have to diffuse laterally to a p-type strip. The high degree of correlation between the LBIC measurement and the Sentaurus model further confirms the validity of the determination of the front surface recombination velocity at 80 cm/s.

## 5 EFFICIENCY POTENTIAL OF INTERDIGITATED BACK HETEROJUNCTION

Sentaurus modelling was used to estimate the efficiency potential of the IBC silicon heterojunction device. Using the present technology and device dimensions, from section 3.3 (Figure 4), an efficiency of 22.7% can be reached in the near term. Further increases in efficiency will be obtained by optimising the device dimensions. For instance, by reducing n-strip width to 200  $\mu\text{m}$  (the limit of, for example, screen printing) with fixed total sum of p- and n-strip based on Figure 5,  $J_{SC}$  can be increased and the efficiency will be enhanced to 23.6%. Since the junction is at back surface for IBC-SHJ cell, the thinner wafer thickness would give higher current due to less carrier recombination in the wafer, but light trapping will be required. Finally, the material properties of a-Si layers used in simulation is fit to the experiments, and might not be ideal. Further optimization to the a-Si properties could also improve the cell performance. In accounting all the above, an efficiency over 24% can be expected for IBC-SHJ solar cells.

## 6 CONCLUSIONS

Interdigitated back contact solar cells using heterojunctions are a potentially low cost method for fabricating high efficiency solar cells. Present devices show a high voltage of 691 mV but low fill factors limit performance. Devices show little shunting between the n and p regions. Further device performance improvements are expected through the use of thinner wafers, texturing and the optimization of the i-layer deposition profiles.

## 4. ACKNOWLEDGEMENTS

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